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Design of M-tree Adder using majority logic for removal of artifacts in bio signal

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ABSTRACT

This research's motivation has focused on signal processing in VLSI design for improving the system throughput in terms of high performance, energy-efficient, high speed, and small chip area. Very Large Scale Integrated circuit plays a vital role in modern technologies. The technology improvements happened because a general digital system design's processing device faces ethical challenges for intricate circuit design. In the recent era, the VLSI has the most compact and powerful IC fabrication technique to improve an individual processor's efficiency. This chapter stretches the design of digital circuits such as binary adders, multipliers, and implementation of FIR in signal processing, which is associated with a novel algorithm for the removal of power line interference in the bio-signal application. Also, deal with the current trends to identify the various pipeline architecture design and algorithms to bring out an optimized solution using a modern analytical method to improve the processor speed and accuracy. The proposed adder has achieved 96% efficiency in terms of gate count, delay, and power compared with existing analysis. Digital system design produces 83.5% efficiency in an existing system and it required the maximum number of gate count and an increasing number of delays when compared with recent research. The design summary is analyzed by using XILINX 14.7 ISE synthesis and the implementation process is highly reached with the help of MATLAB 2018a. IC fabrication is the most important design process in today's VLSI manufacturing industry. Application of SOC is used to fabricate more chips with the help of silicon resonator, to accomplish the circuit complexity by using silicon resonator which is more suitable for the fabrication process and reducing manufacturing cost.

1. Introduction

Motorola invented the integrated circuit in the 1950s to find a solution for the existing scaling factor. A million numbers of logic circuits are interconnected on a single chip by using IC [1]. The IC's are classified into different categories with the help of scaling integration, which is labelled in Small Scale Integration (SSI) is an initial integration process to fabricate a small number of transistors on a chip [3]. The transistor contains a hundred logic gates on a chip to be applied only on small area applications. For extensive area interconnection on fabrication needed the multiple numbers of small-scale integration, consider the designer requirements, the medium-scale integrated circuit is implemented. This scaling range between thousands of transistors is built on a chip. In addition to that, increasing the processor speed, large-scale integration was initiated. [8] It is challenging for the IC implementation process to use breadboard connections. Due to the board connection, the fabrication system occupies more area, power, and delay. An advanced method is developed with the source of computer-aided design. It is one of the very fast-moving technology to analyze and improve system efficiency.[12] The designer can design and analyze a million transistors in a fraction of seconds using digital VLSI design. It is beneficial to understand the design concept in the easiest way by using design hierarchy and improving efficiency, reducing the circuit complexity and interconnection problems. This paper discussed the conventional and pipelined architecture of adder and multiplier. The logical adder design style carries propagation to send the binary data from one block to multiple blocks. The critical path delay creates a large issue when switching the binary data from one place to another. A digital adder is [18] required to design a binary multiplier for various applications such as removing power line interference in a digital filter,

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signal processing, image processing, adaptive and optimized filter design, etc. The system's quality can be described by area, delay, and system cost, which survey in a review paper. The adders are classified into Carry save adder, Carry look-ahead adder, Carry skip adder, and Carry select adder. Technology improvement of these adders is having efficient scaling to achieve low power, area-efficient, and high-speed architecture. Super perfection of pipelined carry-save adder[20], anticipated designing a flawless multiplier. Carry save adder is a fast unconditional adder used to reduce size, power, and delay compared with other conventional adders. several structures are used for optimized filter design. The multiplier is mostly a wanted and dedicated source for any processor to increase system design. Using a modified carry save adder, the pipelined multiplier was designed, the detail of the chosen multiplier is compact and more productive, which was discussed in the literature survey. For the fast-moving processor, a multiplier leads the cradle to design various effective architecture designs for the digital signal processor, microprocessor, etc.,[3] by developing multiple algorithms and architecture to overcome the deficiency system design. Optimization of area, power, and delay is achieved by using a pipelined multiplier.The conventional multiplier is related to the pipelined multiplier. From the observation using advanced architecture, the portable compact processor [5] was designed. The Wallace tree multiplier's essential operation, and it was developed by using two operands: multiplicand and multiplier. Two operands are multiplied by using binary logical AND operation. Due to the multiplication of binary values, the partial product term was generated. The addition process was then done with various adders, which depends on the efficiency of system performance. Depending upon the requirement of applications, a multiplier is chosen to speed up the system operation. In general, the multiplier elements are divided into two parts that are serial/parallel architecture. The result was analyzed and segregated into two parts that are partial product generation and accumulation. Resourceful digital operations are needed for good logic gates to design arithmetic and logical IC fabrication units in low-power VLSI design[10]. The high-speed system's performance is an immense trial to create an enormous amount of controllability and a compact processor or architecture for low power, multimedia, signal processing applications, etc. Energy consumption is more critical for signal processing operation. More research was done in arithmetic logic design. A digital adder is a significant resource for all digital signal processing and communication applications. In the VLSI circuit, the binary adders are essential[11]. Innovative carry propagation and the sum of each adder operation are effective ways to accomplish and reduce the circuit complexity and power between each stage of the addition operation Reduction of circuit complexity is a significant issue in practical implementation because of involving all input bits. The fundamental arithmetic operations in a digital circuit, such as binary addition, binary subtraction, binary multiplication, and binary divisions, are vital elements in signal processing. The complex adders are possible with the help of half adder and full adder, and adders play a crucial role to determine the efficiency of hardware circuits. The digital system addition of two operands is most frequently used [15], and also it can perform functions like multiplication, division, increment, and decrement. As a part of different characteristics, some adders, such as ripple carry adder, have to perform the slowest addition operation because of late responses of carry signal from each stage. The computational time can be optimized with the help of carry select adder and carry skip adder leading to increased area and power. High energy consumption is required for a fast carry look-ahead adder, and this adder occupies more space than other adders. Among the above characteristics of each adder has some demerits depending upon application requirements. The carry-save adder is proposed to design an effective, more compact, suitable, and less powerful pipeline architecture. [6] A modified full adder is proposed. The existing adders lead to higher trade-offs due to wide variations in area, speed, and power. [13] Therefore, one of the parameters has to be optimized to manage the design trade-off and expand the design space mixed adder has been introduced. It consists of carry-in and carry-out signals and is used to design more an adder with optimized delay and power. In data path enhancing, an adder is one of the essential blocks, the data path unit which is present depends upon the implementation of DSP and some other computer applications.

The majority logic-based carry save adder and carry look-ahead adder is introduced in Ref. [18], this majority logic needs more number of Xor gate to analyze the carry select adder as well as it required more number of the gate to analyze the carry save adder. From the analyzes, this technique consumes high circuit complexity, and the delay also high due to the increasing number of gates.

From the overall analysis, this proposed system based on a digital level approach [20], and it is used to design a modified carry save adder by using majority logic. The pipelined architecture design is implemented into a digital filter using the proposed adder, and the designed filter characteristic is applied to signal to process. The real-time application for IC fabrication is analyzed by using the proposed carry save adder with a ring resonator. This free spectral range resonator is used to produce an effective and well-defined fabrication process, compare other resonator proposed system reached less circuit complexity and accuracy is more.

2. Exploring the various adders characterization

2.1. Half adder

The half adder is the most basic. It has the same weight of input and output signal for arithmetic operation. The expression & truth table for half adder is given below,

$$Sum = a \oplus b \tag{1}$$

$$Carry_{out} = a\&b \tag{2}$$

2.2. Full adder

The basic adder function using three input variables is represented in the name of the full adder. The simple structure of half adder having two inputs to operate. It is sufficient only for a simple circuit. For large architectural design, it has consumed more area. So the drawback of half adder is overcome by a full adder. The full adder also generates [3] SUM and CARRY with the help of binary expression SUM will be generated by using a three-input XOR gate, CARRY will be generated by using AND gate. It consists of 1 XOR gate, 3 AND gate, and 1 OR gate. It performs only the addition of single-bit numbers. The addition of n bit numbers is not possible in the full adder.

$$C_{out} = (a * b) + (b * cin) + (a * cin) \tag{3}$$

$$\mathrm{S} = \mathrm{a} \oplus b \oplus cin \tag{4}$$

2.2.1. Classification of adders

Based on the system-level approach, the basic adder is classified into some other adder, which depends on the system requirement. From the evaluation, the binary adder is characterized into.

- Carry skip adder
- Carry select adder
- Ripple Carry adder
- Carry look-ahead adder
- Carry save adder

An analysis report shows the better performance [4] of the majority logic method which is implemented into carry save adder design by using synthesis and simulation tool (see Fig. 1).

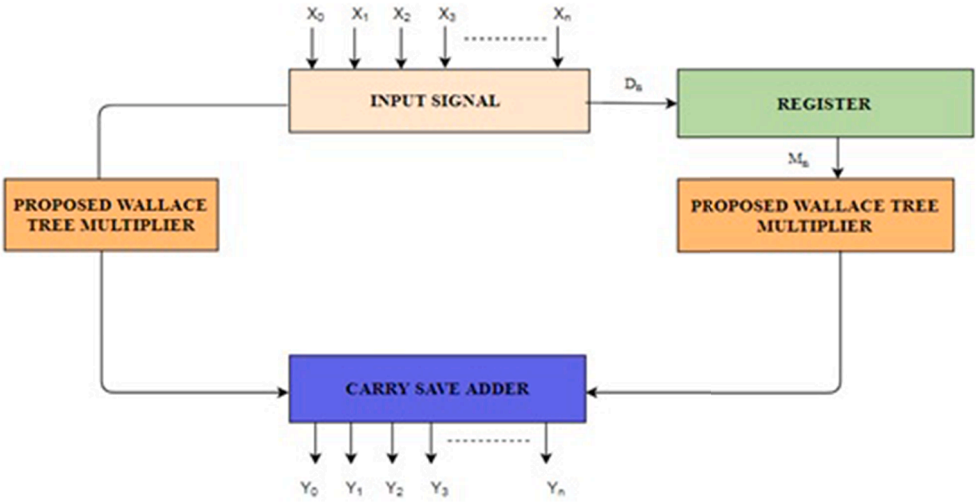

Fig. 1. Functional block diagram of System-level approach.

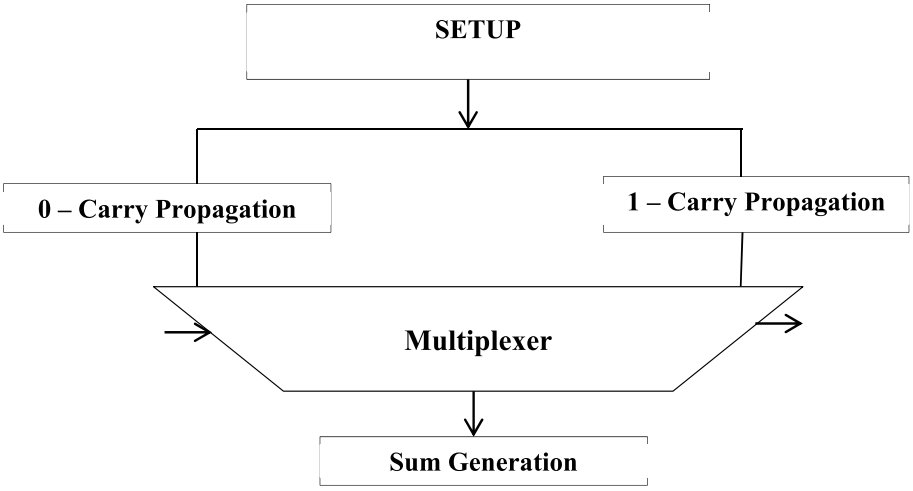

Fig. 2. Carry select adder.

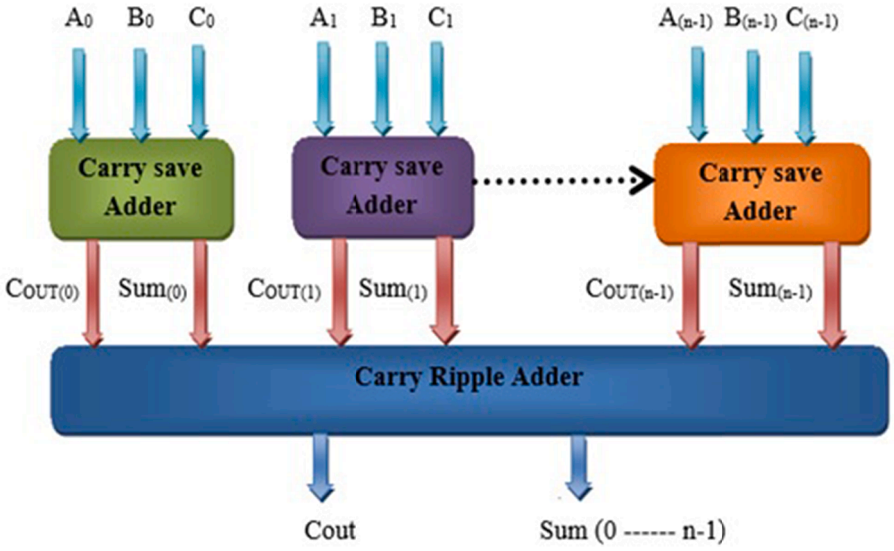

Fig. 3. Carry save adder.

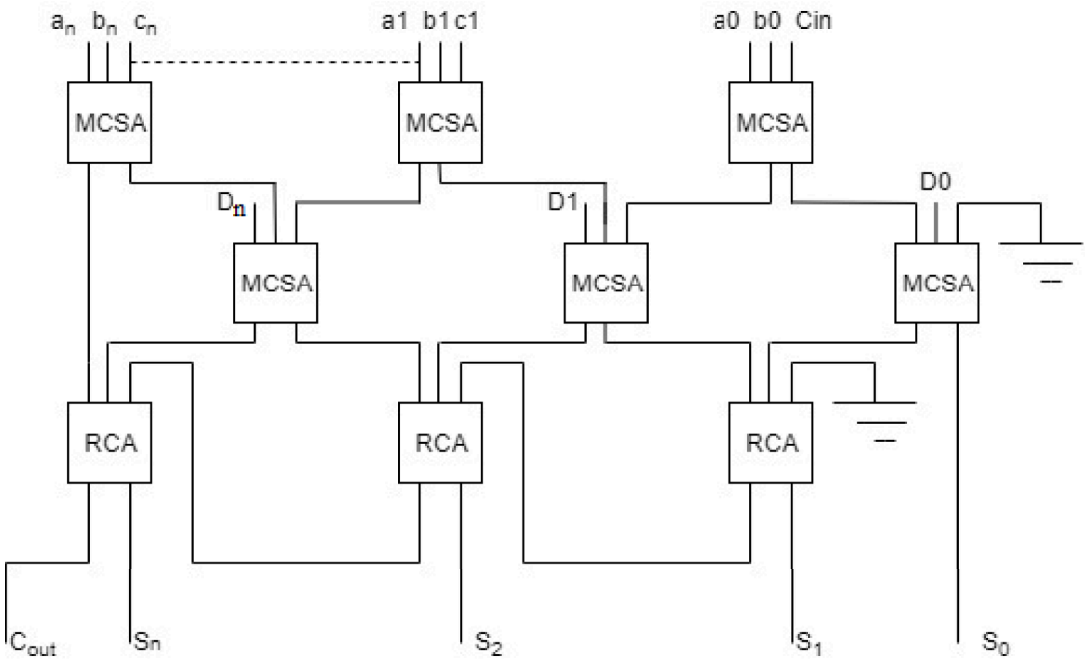

Fig. 4. Modified carry save adder.

2.3. Carry select adder

The carry select adder is used for a more comprehensive addition operation. The addition of two n bit numbers is grouped into two groups report as a conditional carry select (CCS) adder circuit with a multiplexer to select the signal, suitable for low power VLSI implementation. It is considered one of the perfect adders for the suitable rich process and carries out the digital circuit's arithmetic operation. The carry select adder is combined with a multiplexer and produces the final output. From the analyze the optimized method prerequisite more area to design an efficient structure. In the wise of cost and performance in adder design, the CSA method is appreciable in the tradeoff. In Fig. 2 Shown binary carry input and ripple carry adder and one multiplexer (see Figs. 3 and 4).

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- Carry select adder is used to reduce propagation delay
- Low power consumption
- Less complexity

2.4. Carry save adder

It has similar behavior like full adder but it is used to perform n number of bits at a time. The working operation of carry save adder is used to perform simultaneous parallel addition operation. It has more efficient when compared to other adders because of power consumption, easy to design, and less delay to implement in a large circuit.

2.5. Ripple carry adder

The Ripple Carry Adder is the simplest adder to design the addition of two N-bit binary digits (where N is a positive integer). Ripple Carry Adder is a mixture of full adders in which the carry output acts as an input to the next full adder in a cascade manner. The sixteen carry save adder circuit's connection forms 16-bit Ripple carry adder in a diagrammatical form shown in Fig. 3. The RCA speed process is slow. Hence, the function will remain in the same state until the completion of the carry out operation. The expression for carry ripple adder is,

- All adders cannot work simultaneously. Each adder waits to operate until getting the input from the previous adder output. This causes delays. Thus, the propagation time is high. Due to this reason, this adder is extremely slow.
- It became worst when the n value increases.

2.6. Carry skip adder

The Carry Skip Adder (CSKA) is also known as Carry Bypass Adder [9] Carry Skip Adder's work is to check the input bits set whether it has carry output or not. The CSKA is accomplished by organizing the group to propagate the signal to analyze the group to carry input, whether it will propagate the group to the carry output. The mux's selection line is the simple propagate signal which has to elect from carry input or carry the production. Carry skip cascaded into four full adders, each full adder comes out with a carryout, propagation signal, and sum, but the sum is not shown here. No extra hardware cost in the propagate signal from the full adder was calculated from sum logic. All the propagate signals should be asserted for the carry-out to equal the carry-in. If that was true, the carry input will skip all the past full adders and equal the carry output. In case the propagate group is 0, then at least one of the propagate signals will be 0.

$$PCSKA_{group} = p0{*}p1{*}p2{*}p3 \tag{5}$$

$$Carryout_{CSKAgroup} = Carryin_{CSKAgroup}{*}PCSKA_{group} \tag{6}$$

Table 1
Truth table of Carry Look ahead Adder.

Input			Output					
Carry in	A	B	Carry out	Sum	G	K	P	Carry status
0	0	0	0	0	0	1	0	Delete
0	0	1	0	1	0	0	1	Propagate
0	1	0	0	1	0	0	1	Propagate
0	1	1	1	0	1	0	1	Generate/Propagate
1	0	0	0	1	0	1	0	Delete
1	0	1	1	0	1	0	1	Propagate
1	1	0	1	0	1	0	1	Propagate
1	1	1	1	1	1	0	1	Generate/Propagate

Table 2
Truth table of Modified carry save adder using majority logic.

INPUT			INOUT			OUTPUT	
A	B	C_{i+1}	C_{i-1}	D_{i-1}	M(w_i)	S_i	C_i
0	0	0	1	1	0	0	0
0	1	1	0	0	0	1	1
1	0	1	0	0	0	1	1
1	1	1	0	0	1	1	1

Table 3
Design summary of various 16*Bit Adders.

List of Adders (16 BIT)	No of Slices	Power	Delay
Ripple Carry Adder	24	1436μw	21.69ns
Carry Lookahead Adder	18	1560μw	21.65ns
Carry Skip Adder	37	1760 μw	23.217ns
Carry Select Adder	26	850 μw	15.863ns
Conditional Sum Adder	15	830μw	10.487ns
Proposed Carry Save Adder 1	24	760μw	13.203ns
Proposed Carry Save Adder 2	16	718μw	6.206ns

2.7. Carry look ahead adder

In parallel addition, the overall delay has been decreased by using various types of methods named Carry Look Ahead Adder, which can solve the problem in the carry delay with the input signal's help by watching the signals process. Cultivate a simple RCA with knowledge of costly hardware architecture and complex methods. A carry look-ahead adder digital design t is used to speed up the calculation proposed by Ling. Ling's approach is based on propagating a composite term in place of the conventional carry look-ahead.

$$G_i = A_i * B_i \tag{7}$$

$$K_i = \overline{A_i} * \overline{B_i} \tag{8}$$

$$P_i = A_i \oplus B_i \tag{9}$$

$$S_i = P_i \oplus C_i \tag{10}$$

$$P_i = a_i \oplus b_i \tag{11}$$

$$C_{t+i} = a_i * b_i + b_i * c_i + a_i * c_i \tag{12}$$

- It generates the input carry of each full adder simultaneously.
- It reduces the propagation delay.
- It involves complex hardware and also costlier.
- It became more complicated when no of bits increased.

2.8. Modified carry save adder (proposed adder: 1)

The proposed adder has more efficient when compared with other approximate adders like carry save with carry look-ahead adder, carry save with carry skip adder, etc., the reason for choosing carry save adder with ripple carry adder is low power and less delay compared with other hybrid adders. In this paper [8[the comparison and efficiency are shown in the comparison Table 3. In general, carry save adder has good performance and less complexity. To combine carry save with ripple carry adder it will act as a multiplier. It is more efficient when compared with the Wallace tree-structured multiplier. This modified adder required 4 carry save adder and 1 ripple carry adder which means it required 15 -Xor gate, 16 - AND gate 14 - OR gate for carry save addition operation (see Table 1).

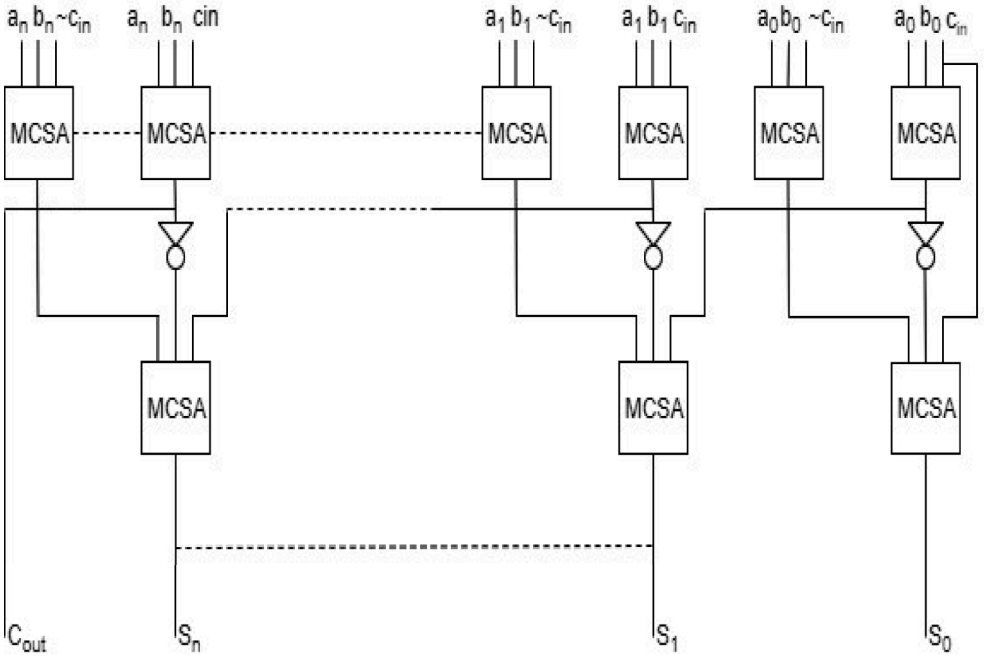

Fig. 5. Modified carry save adder using majority logic.

Project File:	mj_bit.xise	**Parser Errors:**	No Errors
Module Name:	mj_15bit	**Implementation State:**	Placed and Routed
Target Device:	xc3s500e-5pq208	**•Errors:**	No Errors
Product Version:	ISE 14.7	**•Warnings:**	No Warnings
Design Goal:	Balanced	**•Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**•Timing Constraints:**	
Environment:	System Settings	**•Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	32	9,312	1%	
Number of occupied Slices	16	4,656	1%	
Number of Slices containing only related logic	16	16	100%	
Number of Slices containing unrelated logic	0	16	0%	
Total Number of 4 input LUTs	32	9,312	1%	
Number of bonded IOBs	50	158	31%	
Average Fanout of Non-Clock Nets	3.16			

Fig. 6. Design Summary of majority carry save adder.

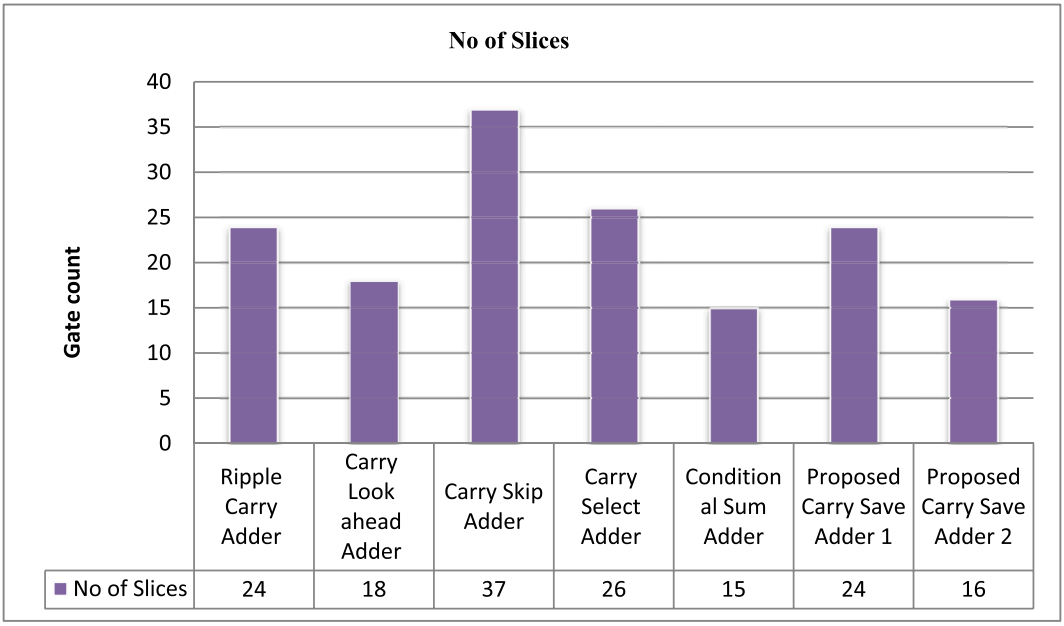

Fig. 7. Summary of carry save adder slice count.

2.9. Modified carry save adder using majority logic (proposed adder: 2)

This proposed carry-save adder has a pipeline structure [7] which has a better performance compared with other conventional and hybrid adder. It has a unique linear optimization design to execute high efficient design process, so the pipelined structure has a separate functional block to avoid interference and increase the system performance. The working function of this circuit has a majority-based carry-save adder. The reason for choosing this adder has to produce only the majority of output from the given binary input. Feature of this adder doesn't require ripple or carry skip adder for processing this system, the carry signal is moved to next stage with the support of wires, and only in the final step, the carry signal is generated C_{out}.

$$C_i = M(A_i, B_i, C_{i+1}) \tag{13}$$

$$S_i = M(M(A_i, B_i, C_{i-1}), w_i, D_{i-1}, C_i) \tag{14}$$

The above Table 2 is a truth table of 2:2 module majority logic-based adder design analysis report with the help of binary inputs. This is a new digital logic system to generate sum & carry using carry input & inversion operation. Carry signal is mandatory for any addition operation, by using this majority logic algorithm which follows.

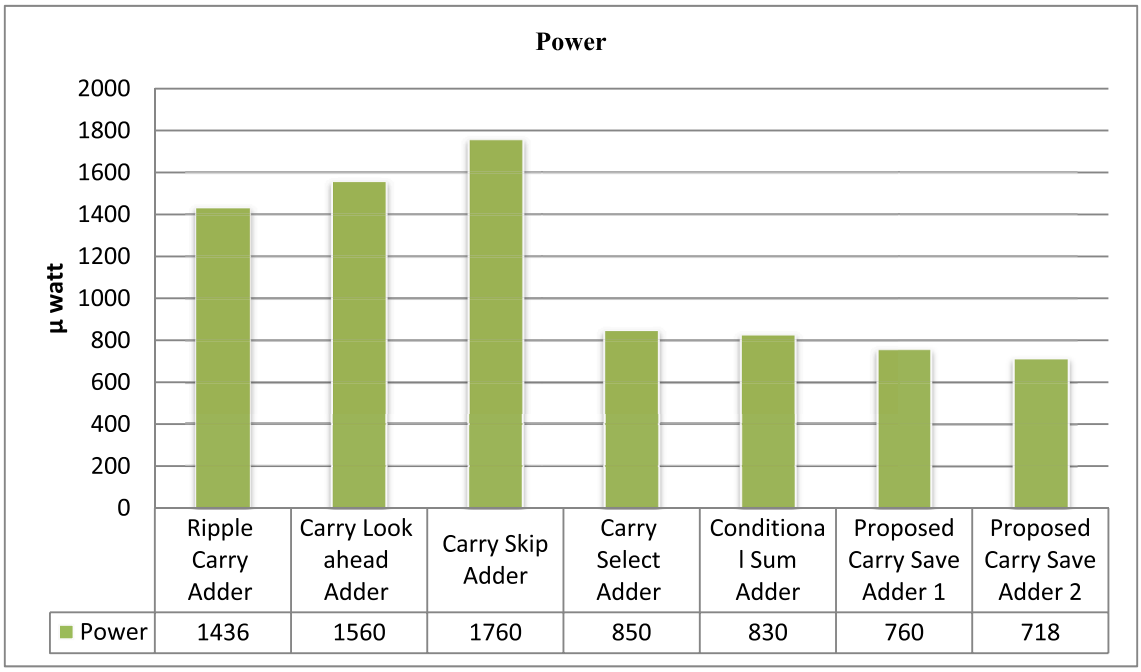

Fig. 8. Power consumption of proposed carry save adder.

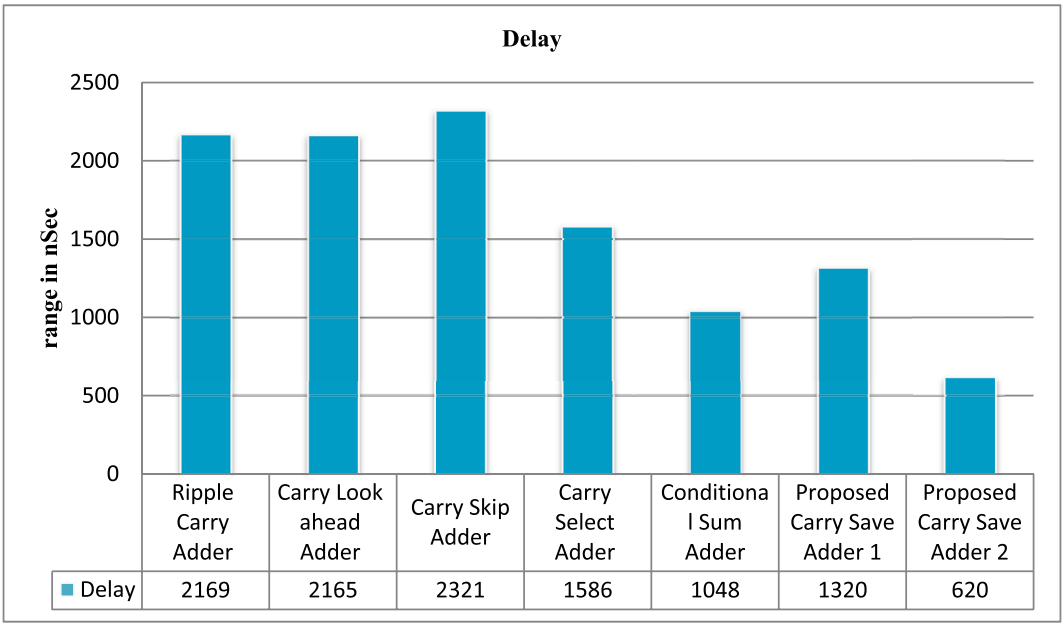

Fig. 9. Usage of delay in proposed carry save adder.

- Easy to reduce circuit complexity with the help of carry save technique
- Reduce delay by using carry in & inversion technique
- Increase speed & reduce memory using the ML algorithm.

The above Table 3 shows the comparison of overall adder performance and its efficiency. To design on efficient architecture in any circuit such as area, power, delay, and memory usage is the most important factor to get an optimal result, behind the reason the proposed majority logic (ML) structure is designed and compared with various classifications of adders (see Fig. 5).

Fig. 6 shows the design summary of 16-bit majority carry save adder, this adder required less number of gate count and occupies a minimum number of LUT when compared with other analysis. from the summary report, the majority carry save adder has occupied slices 16, 4 input LUTs 32, and the number of bonded IOBs 50 (see Figs. 7–9).

3. Case study

3.1. Silicon resonator for CMOS IC fabrication

Real-time examples of CMOS IC fabrication using silicon resonator is a promising application for many system designs such as filters, biosensors, and light sources. The efficient design technique [17,19] is achieved with the help of a ring resonator with a free spectral range process for large scale optimization.

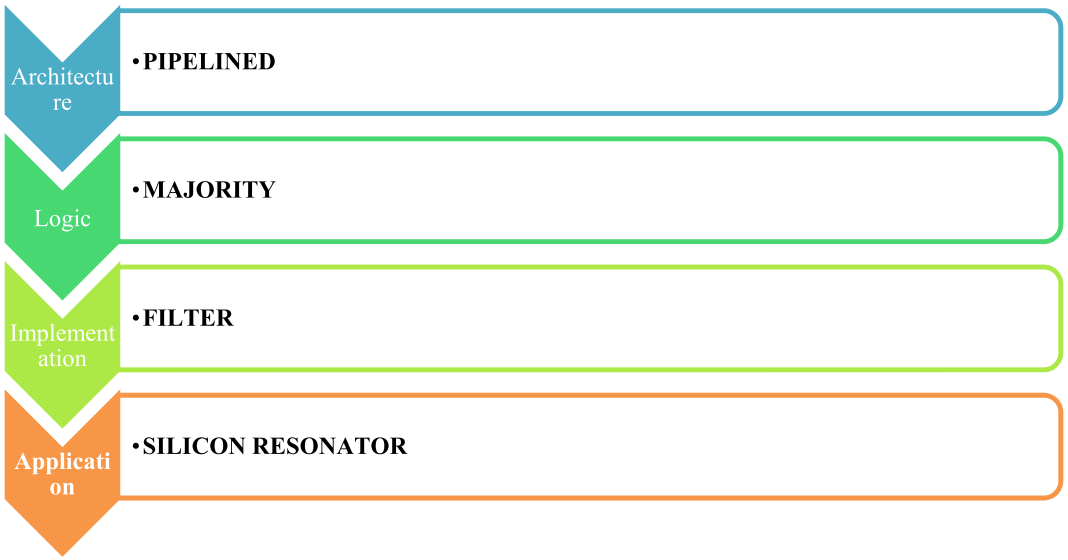

Fig. 10. Functional diagram of Silicon resonator.

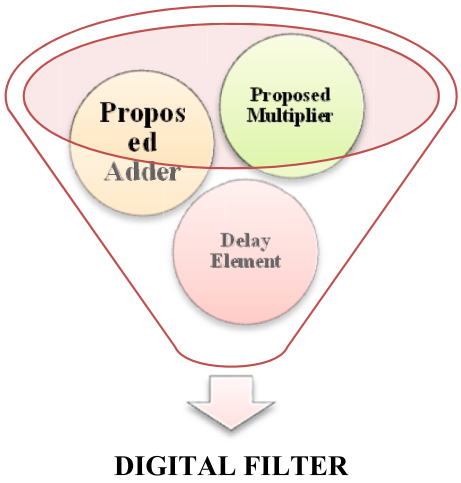

Fig. 11. Functional diagram of digital filter.

In analog, the major resource of microelectronics is designed with the help of more electronics system design and various design techniques for circuit optimization, which is studied using FSR in the different fabrication processes. The upcoming growth of fabrication is analyzed by using a silicon resonator, it is suitable for circuit minimization and accurate analog design. Various kinds of silicon resonators are proposed, based upon the applications this design technique is used to produce a more accurate result when compared with existing system design (see Fig. 10).

4. FIR filter structure

Filter design is a major resource for all signal processing, image processing applications. The overall performance of every individual system is perfectly designed 16by supporting the device of a digital filter. The overreaching of the digital processor in the digital world is proposed by using the digital FIR filter based on ML algorithm, intensified the signals in digital system is a big challenge for all researchers. The modified carry save & carry-in, inversion algorithm has progressively improved the digital FIR filter [17,20] in the new system design process. The efficiency of existing and new design techniques is shown in Fig. 11 which has a simple design of FIR filter, Fig. 12.shows the functional diagram of digital FIR filter design. The performance is evaluated by using the Xilinx ISE simulation tool.

5. Conclusion

In the VLSI area, delay and power are valuable factors for improving system performance. The architecture design concludes that the pipelined carry-save adder architecture design has interconnected, high speed, and low power consumption compared with other adders. From the evaluation, the selected proposed adder signal has a higher resolution compared with other conventional adders, which is used in multiplier design to speed up the system performance. Even though a million design sources are available for increasing digital circuit performance,

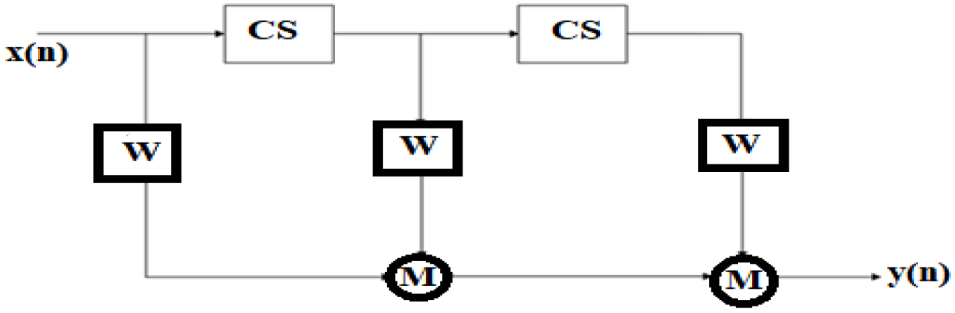

Fig. 12. FIR filter structure.

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	1,051	9,312	11%
Number of 4 input LUTs	422	9,312	4%
Number of occupied Slices	723	4,656	15%
Number of Slices containing only related logic	723	723	100%
Number of Slices containing unrelated logic	0	723	0%
Total Number of 4 input LUTs	422	9,312	4%
Number used as logic	38		
Number used as Shift registers	384		
Number of bonded IOBs	14	232	6%
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	1.84		

Fig. 13. Modified Carry save FIR Filter Design summary.

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	1,042	9,312	11%
Number of 4 input LUTs	221	9,312	2%
Number of occupied Slices	624	4,656	13%
Number of Slices containing only related logic	624	624	100%
Number of Slices containing unrelated logic	0	624	0%
Total Number of 4 input LUTs	221	9,312	2%
Number used as logic	29		
Number used as Shift registers	192		
Number of bonded IOBs	8	232	3%
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	1.90		

Fig. 14. Majority gate based FIR Filter Design summary.

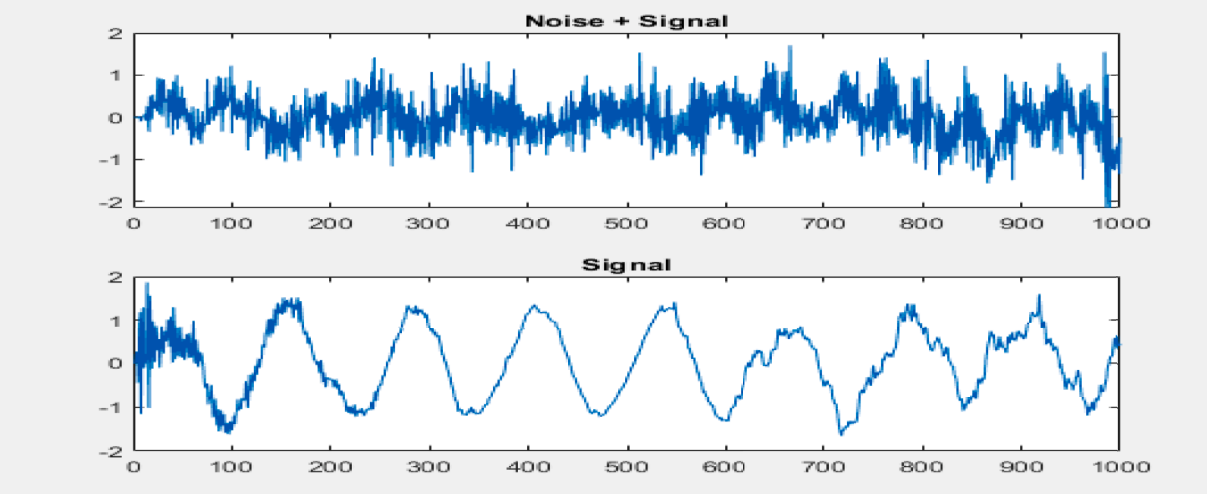

Fig. 15. Majority carry save adder in FIR filter output.

multipliers have a significant role to increasing system performance. The modified carry-save adder intention is to implement in the conventional and pipelined multiplier for efficient design. The efficiency of this design process is summarized with the help of the Xilinx ISE 14.7 simulator. The execution and comparison result is shown in Figs. 13–16. The overall performance in terms of percentage for ML-based carry save FIR filter design reached 86% when compared with modified carry save FIR filter design. This proposed system can design using Majority logic with the help of a QCAD designer. A majority is an advanced system design process in terms of a cell-based design circuit. The Majority logic is a fast computation method in any applications for increasing system performance. This is a more satisfying technique in the quantum Dot Cellular

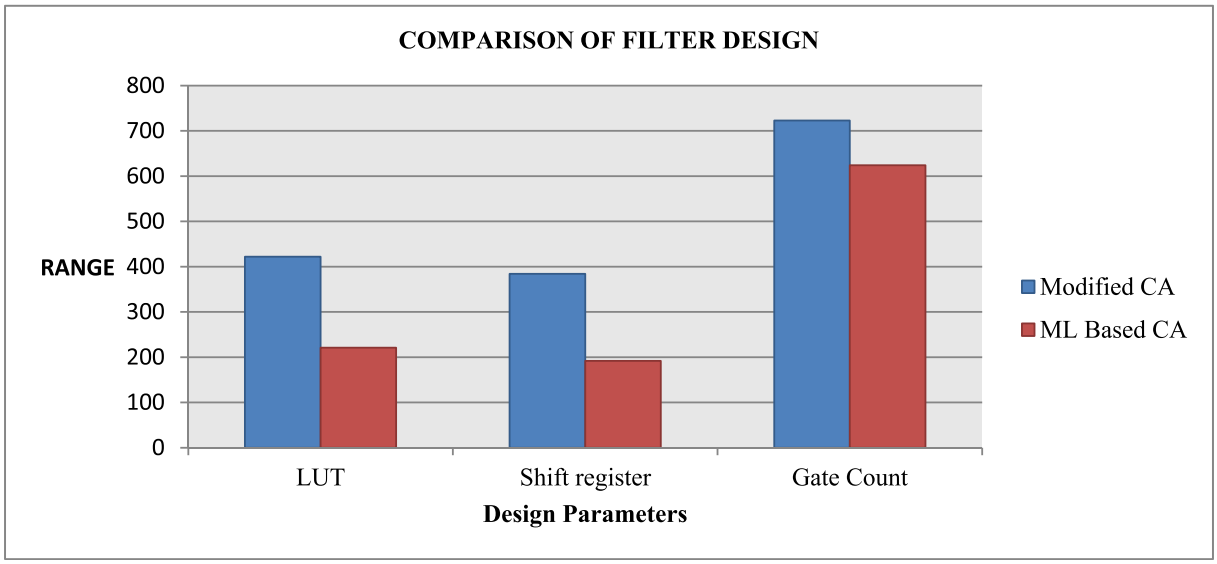

Fig. 16. Comparison of ML & modified carry save FIR filter design.

automata design process. Using majority logic, the proposed system can design in more quickly for fast processor design operation.

Author statement

The corresponding author is responsible for ensuring that the descriptions are accurate and agreed by the co-author.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mejo.2020.104901.

References

[1] J.-P. Deschamps, G.J.A. Bioul, G.D. Sutter, Synthesis of Arithmetic Circuits: FPGA, ASIC, and Embedded Systems, Wiley, 2006.
[3] M.A. Karim, C. Chen, Digital Design: Basic Concepts and Principles, CRC Press, 2008.
[4] S. Brown, Z. Vranesic, Fundamentals of Digital Logic with VHDL Design, third ed., McGraw Hill publishers, 2009.
[5] Hamid MM. Kamboh, Shoab A. Khan, FPGA Implementation of Fast Adder, in: International Conference on Computing and Convergence Technology, IEEE Press, 2012, pp. 1324–1327.
[6] R. Vimala, K. Baskaran, K.R.A. Britto, Modeling and filter design through analysis of conducted EMI in switching power converters, Journal of Power Electronics 12 (4) (2012) 632–642.
[7] P. Balasubramanian, D.L. Maskell, A distributed minority and majority voting based redundancy scheme, Microelectron. Reliab. 55 (August–September 2015) 1373–1378.
[8] V.S. Balaji, Har Narayan Upadhyay, An implementation of area and power-efficient digital FIR filter for hearing aid applications, J. Optoelectron. Adv. Mater. 9 (2015) 657–662.
[9] M. Bahadori, M. Kamal, A. Afzali-Kusha, M. Pedram, High-speed and energy-efficient carry skip adder operating under a wide range of supply voltage levels, IEEE Trans VLSI Syst (2016) 421–433.
[10] Aravind Britto, A novel analyzation method for predicting health condition based on ECG healthcare big data using a probabilistic data compilation method, Perspect. em Cienc. Inf. 22 (1) (2017) 1–13.
[11] R. Katreepalli, T. Haniotakis, High speed power efficient carry select adder design, in: Proc. of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI-2017), July-2017, pp. 32–37.
[12] K.R.A. Britto, et al., Preprocessing and Signal Processing Techniques on Genomic Data Sequences, Biomedical research, 2017.
[13] A. Dalloo, A. Najafi, A. Garcia-Ortiz, Systematic design of an approximate adder the optimized lower Part Constant-OR adder, IEEE Trans VLSI Syst (2018) 1595–1599.
[15] F. Jafarzadehpour, A.S. Molahosseini, A.A. Emrani Zarandi, L. Sousa, New energy-efficient hybrid wide-operand adder architecture, IET Circuits, Devices Syst. (2019) 1221–1231.
[16] Martina Ladrova, Radek Martinek, Jan Nedoma, Marcel Fajkus, Methods of power line interference elimination in EMG signals, Journal of Biomimetics, Biomaterials, and Biomedical Engineering 40 (2019) 64–70.
[17] Basant Kumar Mohanty, et al., A high-performance FIR filter architecture for fixed and reconfigurable applications, IEEE Trans. Very Large Scale Integr. Syst. 24 (2) (2016).
[18] Sarvarbek Erniyazov, Jun-Cheol Jeon, Carry save adder and carry look-ahead adder using inverter chain based coplanar QCA full adder for low energy dissipation, Microelectron. Eng. (2019) 37–43.
[19] Boling Ouyang, Yufei Xing, Wim Bogaerts, Jacob Caro, Silicon Ring Resonators with a Free Spectral Range Robust to Fabrication Variations, vol. 27, OSA Publications, 2019. Issue 26.
[20] S. Aathilakshmi, K.R. Aravind Britto, Digital filtering using multipliers on intelligence extraction and power-line removal from electromyogram signals, Journal of Medical Imaging and Health Informatics 10 (2020) 30–37.

Further reading

[2] Uwe Meyer-Baese, Digital Signal Processing Using Field Programmable Gate Arrays, Springer-Verilog Berlin Heidelberg, 2007.
[14] M. Pashaeifar, M. Kamal, A. Afzali-Kusha, M. Pedram, Approximate reverse carry propagate adder for energy-efficient DSP applications, IEEE Trans VLSI Syst 16 (11) (2018).