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Research Article

A performance Analysis of DM-DG and TM-DG TFETs Analytical Models for Low Power Applications

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Abstract: Device Modeling is utilized to engendering incipient device models for the demeanor of the electrical devices predicated on fundamental physics. Modeling of the device may also include the creation of Compact models. An emerging device type of transistor is the Tunnel Field-Effect transistor that achieves compactness and speed during device modeling. This article presents an analytical comparative study of duel material DG TFETs and triple Material DG TFETs with gate oxide structure . Here the implementation of device modeling is done by solving Poisson's equation with Parabolic Approximation Technique(PAT).The process of formulation of drain current(Id) model is based on integrating the BTBT generation. A Transconductance model of the device is additionally developed utilizing this drain current model of TFET. Surface potential is calculated by utilizing the channel potential model. The electrical properties like Surface potential⟦(Ψ⟧_(s,i)), Drain current (Id), and Electric field(Ei) have been compared for both Duel material DG-TFET and Triple material DG-TFET. The comparison statement of DMDG-TFETs and TMDG-TFETs provide improved performance. The analytical model of the device results are compared with simulated results for DMDG TFET and TMDG TFET and good acquiescent is examined.

Keywords: Parabolic Technique, Tunnel FET (TFET),Band-to-band tunneling (BTBT),Triple Material(TM), Double Gate(DG), Dual-Material(DM), Work function.

1. Introduction

As we scale down the MOSFET to sub-30 nm administration, deals with the major complexity and noteworthy challenges. For extreme low power applications, it confronts key difficulties and paramount challenges in the engendering of incisive doping slope at the source and depletes intersection. Poor electrostatic control and decreased short channel conduct of routine MOSFET offers ascend to the low esteem of depleting incited hindrance bringing down and high spillage current in OFF state. Downsizing the supply voltage and limit voltage is a noteworthy supporter of the sub-threshold spillage which prompts over top power utilization. The constraint in sub-threshold slant because of Fermi-Dirac dissemination of vitality turns into the bottleneck for further scaling of the supply voltage. Low estimation of SS gives a lower sub-threshold spillage which additionally offers ascend to low power dissemination. An ordinary MOSFET can't conquer this hypothetical constraint because of its float dissemination component of current conduction. Over the most recent couple of decades, option transistors have been proposed to accomplish Sub-threshold(SS) lower than 60 mV/decade at room temperature, in light of low power request. The most usually detailed among option transistors is the passage field impact transistor [3, 4], which does not endure from SCEs because of its diverse conduction instrument. In spite of the fact that routine TFET has better Sub-threshold(SS) than reversal mode (IM) gadget, it has low ON-current what's more, creation gets to be distinctly testing in sub-30 nm area for both TFET and IM gadget. A conceivable method for taking care of the issue of low ON-current is the utilization of low band crevice semiconductors like strained silicon, germanium, evaluated SiGe, and utilization of III–V materials like GaAs, InAs [5–7], and so on. All things considered the creation of strained silicon and reviewed SiGe is not good with standard CMOS handle stream and likewise, because of tight band hole OFF state band to band burrowing (BTBT) rate increments and thus offers poor ON current to the OFF-current proportion. As Tunnel FETs being the most promising device for low power applications, it caters more benign than FETs. The most resolvable constraint of Tunnel FETs is its low ON-current. The new emerging methods like the Band Gap Engineering ,Gate-Oxide Engineering used to enhance the ON-current and reduces the leakage through the gate dielectric of the TFETs. This is what it refers to that the different electrical characteristics of the Tunnel FETs can be ameliorated significantly by superseding the conventional SiO2 by a stacked gate oxide of SiO2 and a high-k dielectric material in the Double Gate Tunnel FETs. A DMG- TFET was proposed because to mitigate such issues (ie., low ON current) in which the tunneling gate has work function lower than that of the auxiliary gate for n-channel and vice-versa for p-channel of TFET.

Due to enhanced tunneling, DMG-TFETs exhibit upper ON current by a lower work function of metal near-source which gives enhanced I_{ON}/I_{OFF} and Sub-threshold swing(SS). The device model is verified by comparing its results with simulated results obtained from TCAD software with parametric characteristics The On-current(I_{ON}) of the TFETs can be significantly enhanced by adding the Triple Material high-*k* stacked gate oxide in the Double Gate TFETs.

2. Model Derivation

The cross-sectional view of the DM-DG TFET is shown in fig(1). Here L1, L2, and L3 represents the channel length(L1) of DM-DG, Tunneling gate length(L2) of DM-DG, auxiliary gate length (L3) of DM-DG and R1, R2, R3, represents the source/channel depletion region(R1), channel depletion region(R2), and drain/channel depletion region(R3)correspondingly. The sio2thickness, High-K material thickness, and channel thickness are denoted by t_{ox},t_k, and t_{si} respectively. To avoid the lattice mismatch the high-k material has not been utilized directly on the silicon channel as shown in the figure. The x-axes used to indicate the length of the channel and y axes used to indicate the channel oxide denoted thickness respectively.

The potentials of junction are denoted as $\Psi_{0,}\Psi_{1,}\Psi_{2,}and\Psi_{3,}$at

$$x_0 = 0, x_1 = L_1, x_2 = L_1+, \ x_3 = L_1 + L_2 \ + L_3$$

respectively along the channelIn Fig 1, M1 and M2 are the two laterally connected gate electrodes.

The gate electrode near the source is called a tunneling gate (M1)with a work function of 4.2eV and the gate electrode near the drain is called the auxiliary gate(M2) with a work function of 4.0eV.

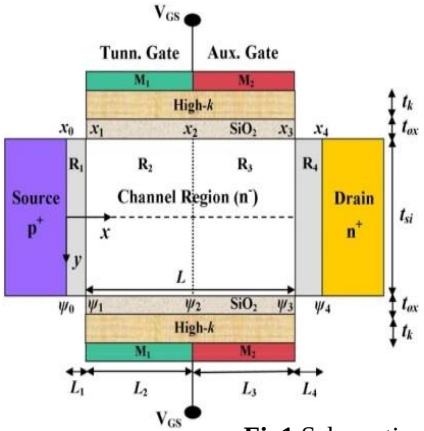

Fig1.Schematic diagram of Duel Material DG-TFET

Let Ψ_0, Ψ_1, Ψ_2 andΨ_3 specifies the junction potential at $x_0, x_1, x_2$and x_3 .

1. surface potential model for DM-DG TFET

The channel can be mentioned using 2-Dimentional equation as

$$\frac{\partial^2 \Psi_i(x,y)}{\partial x^2} + \frac{\partial^2 \Psi_i(x,y)}{\partial y^2} = \pm \frac{qN_i}{\epsilon_{si}} \quad \text{i=1,2,3,4} \rightarrow (1)$$

the 2-Dimentional electrostatic channel potential can be written as

$$\Psi_i(x,y) = \Psi_{0i}(x) + [V_{G,i}^{ref} - \Psi_{0i}(x)]\left(\frac{y}{\lambda_i^2}\right) \qquad \rightarrow (2)$$

Using the parabolic approximation method, The 2-Dimentional electrostatic surface potential can be mentioned as

$$\Psi_{s,i}(x,y) = \Psi_i(x, \pm t_{si}/2)$$

$$= \Psi_{0i}(x) + [V_{G,i}^{ref} - \Psi_{0i}(x)](t_{si}/2\lambda_i)^2 \quad \rightarrow (3)$$

here the Si andλi are the electron affinity and thecharacteristic length respectively.

The characteristic length of the DM-DG TFET in lined with the channel potential is specified by

$$\lambda_i = \left(\frac{C_{ch}}{C_i} + \frac{1}{4}\right) t_{si}^{2}{}^{1/2} \rightarrow (4)$$

εsi,εox, and $\varepsilon k$are the permittivities of the silicon (Si), SiO2, and high-*k* dielectric respectively.

The channel region capacitance expression is

$C_{ch} = \epsilon_{si}/t_{si}$ and C_i={1,2,3,4} → (5)

The expression for channel potential in the device region can be mentioned as,

$$\Psi_{0i}(x) = A_i \exp\left(\beta_i (x - x_{i-1})\right) + B_i \exp\left(-\beta_i (x - x_{i-1})\right) + Q_i \rightarrow (6)$$

The following boundary conditions helps to arrive constants *Ai* and *Bi*

$\Psi_0 = \Psi_1(0, y) = -V_T \ln\left(\frac{N_1}{n_i}\right) \rightarrow$ (7)

$\Psi_1 = \Psi_1(L_1, y) = \Psi_2(L_1, y) \rightarrow (8)$

$\Psi_2(L_1 + L_2, y) = \Psi_3(L_1 + L_2, y) \rightarrow$ (9)

$\Psi_3 = \Psi_3(L_1 + L_2 + L_3, y) = \Psi_4(L_1 + L_2 + L_3, y) \rightarrow (10)$

$\Psi_4 = \Psi_3(L_1 + L_2 + L_3 + L_4, y) = V_T \ln\left(\frac{N_3}{n_1}\right) + V_{DS} \rightarrow (11)$

$$A_i = \frac{-1}{2\sinh(\beta_i L_i)} (\Psi_{i-1} \exp(-\beta_i L_i) - Q_i(1 + \exp(-\beta_i L_i)) - \Psi_i) \rightarrow (12)$$

$$B_i = \frac{-1}{2\sinh(\beta_i L_i)} (\Psi_{i-1} \exp(\beta_i L_i) - Q_i(1 + \exp(\beta_i L_i)) - \Psi_i) \rightarrow (13)$$

$$P_i = V_G^{ref} + \frac{qN_i}{\epsilon_{si}\beta_i^2}, \beta_i^2 = \frac{2}{\lambda_i^2} \rightarrow (14)$$

2. Electric potential for DM-DG TFET

The electric field distribution in the channel is modified such that the field near the source becomes larger causing more rapid acceleration of the electron. Thus the average carrier transport velocity in the Channel is increased, which leads to the enhanced performance of the device.

The expression of electrostatic field can be written as

$$E_{xi}(x, y) = \beta_i \left(1 - \left(\frac{y}{\lambda_i}\right)^2\right) [A_i \exp\left(\beta_i (x - xfa_{i-1})\right) - B_i \exp\left(-\beta_i (x - x_{i-1})\right)] \rightarrow (15)$$

$$E_{yi}(x, y) = y[V_{G,i}^{ref} - \Psi_{0i}(x)]\beta_i^2 \rightarrow (16)$$

3.Drain current model for DM-DG TFET

The Kanes model is used to calculate the band to band tunneling generation rate.

The band to band tunneling generation rate can be mentioned as

$$G_{BTBT} = A_{kane} E^{\alpha} \exp\left(\frac{-B_{kane}}{E}\right) \rightarrow (17)$$

where $A_{kane} = \frac{q^2 m_r^{1/2}}{18\pi\hbar^2 E_g^{1/2}}$ and $B_{kane} = \frac{\pi m_r^{1/2} E_g^{3/2}}{2q\hbar} \rightarrow (18)$

The drain current equation can be mentioned as

$$I_d = \iiint A_{kane} E(x, y) E_{avg}^{\alpha - 1} \exp\left(\frac{-B_{kane}}{E_{avg}}\right) dxdydz \rightarrow (19)$$

The calculation of shortest tunneling path is done by

$$\Psi_{s,2}\left(L_t^{min}\right) - \Psi_0 = \frac{E_g}{q} \quad \longrightarrow \quad (20)$$

$$L_t^{min} = \frac{1}{\beta_2} \ln\left(\frac{R + \sqrt{R^2 - 4A_2B_2}}{2A_2}\right) \quad \longrightarrow \quad (21)$$

where R=$\frac{1}{k}(\Psi_0 - P_2 k - V_G^{ref}(1-k) + E_g/q$ and

K=$(1 - \frac{t_{si}^2}{4\lambda_2^2})$.The drain current derived after the substitution in the various expressions is

$$I_d = I_0\left(\frac{A_2 M_{lt}^{min}}{\chi_1} + \left(\frac{A_3}{\chi_3} - \frac{A_2}{\chi_1}\right) M_{L_1+L_2} * \left(\frac{B_2}{\chi_2} - \frac{B_3}{\chi_4}\right) N_{L_1+L_2} \frac{B_2 N_{lt}^{min}}{\chi_2}\right) \rightarrow (22)$$

$$\chi_1 = \chi_3 = \left(\left(\frac{qB_{kane}}{E_g} - \beta_2\right) \text{and } \chi_2 = \chi_4\left(\left(\frac{qB_{kane}}{E_g} + \beta_2\right)\right.\right. \quad (23)$$

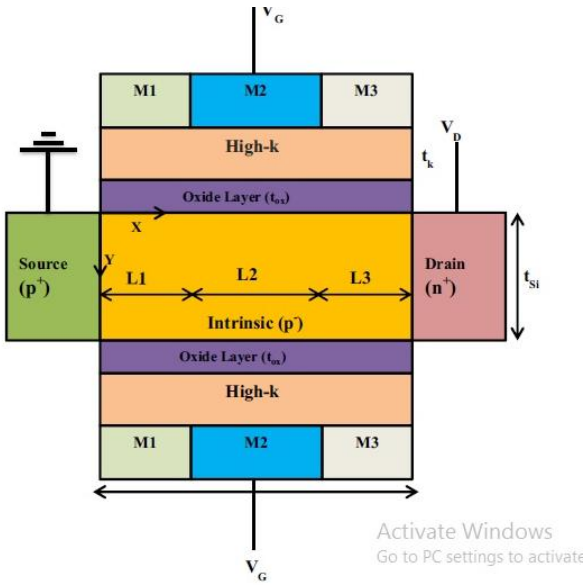

Fig2. Schematic diagram of Triple Material DG-TFET

The cross-sectional view of the Triple Material-DG TFET is shown in fig(2). The channel length is denoted as L. Here *L*1, *L*2, *L*3 are the length of the tunneling gate(L1), control gate(L2), auxiliary gate(L3), *tk*, *tsi*, and *tox* are the thickness of the high-K dielectric, silicon channel, and auxiliary gate length respectively.

1.Surface Potential Model for TMDG TFETs:

The Poisson equation for the two Dimension channel representation is

$$\frac{\partial^2 \Psi_i(x,y)}{\partial x^2} + \frac{\partial^2 \Psi_i(x,y)}{\partial y^2} = \pm \frac{qN_A}{\varepsilon si} \rightarrow (24)$$

εsi and N_A*are* the silicon dielectric constant, channel doping concentration respectively.

In the device channel region the potential profile can be estimated by using a parabolic approximation function

$\Psi(x, y) = \Psi s(x) + C1(x)y + C2(x)y2 \rightarrow (25)$

Where $\Psi s(x)$, *C*1*(x)* and *C*2*(x)* are the Surface potential and the arbitrary coefficient *C*1*(x)* and *C*2*(x).*

$\Psi i(x, y) = \Psi si(x) + Ci1(x)y + Ci2(x)y2 \rightarrow (26)$

In TMDG TFET structure ,the potential under the three gate regions can be written as Ψi where, *i*= 1, 2, 3 .

The following boundary conditions are used to solve Poisson's equation individually in the three gate regions.

For all three metal gates, Electric–flux at the gate oxide interface is continual

$$\frac{\partial \Psi i(x,y)}{\partial y}\Big| \quad y = 0 \; = \; \frac{\varepsilon oi}{\varepsilon si}\frac{\Psi si(x) - \; V^{'}GSi}{teq} \rightarrow (27)$$

For all three metal gates Electric–flux at the gate oxide of the back gate interface is continual

$$\frac{\partial \Psi i(x,y)}{\partial y}\Big| \text{y=tsi} \; = \; \frac{\varepsilon oi}{\varepsilon si}\frac{V^{'}GSi - \Psi Bi(x)}{teq} \rightarrow (28)$$

The surface potential of two different metals at the interface is continual

$\Psi si(x) = \Psi si{+}1(xi\ )$

The electric –flux of two different metals at the interface is continual

$$\frac{\partial \Psi i(x,0)}{\partial x}\Big|\text{x=xi} \; = \; \frac{\partial \Psi i{+}1(x,0)}{\partial x}\Big|\text{x=xi} \rightarrow (29)$$

The source channel potential is Vbi1 = −Eg/2q and the drain channel potential is (Vbi2 +VDS). The arbitrary constants can be obtained from the above boundary conditions.

$$Ci1(x) \; = \; \frac{\varepsilon ox}{\varepsilon si}\frac{\Psi si(x) - V^{'}GSi}{teq} \rightarrow (30)$$

$$Ci2(x) \; = \; \frac{-\varepsilon ox}{\varepsilon si\ tsi}\frac{\Psi si(x) - V^{'}Gsi}{teq} \rightarrow (31)$$

Substituting the above equation, we get

$$\Psi i(x,y) = \Psi si(x) + \left[\frac{\varepsilon ox}{\varepsilon si}\frac{\Psi si(x) - V^{'}Gsi}{teq}\right]y - \left[\frac{-\varepsilon ox}{\varepsilon si\ tsi}\frac{\Psi si(x) - V^{'}Gsi}{teq}\right]y^{2} \rightarrow (32)$$

Surface potentials Ψs1(x), Ψs2(x) and Ψs3(x)in three gate material (M1, M2 and M3) can be obtained by solving the two dimensional Poisson's equation.

$$x^{2}\frac{\mathrm{d}2\Psi si(x)}{\mathrm{d}x2} - \frac{2\varepsilon ox}{\varepsilon si\ tsi\ teq}\Psi si(x) = \frac{qNA}{\varepsilon si} - \frac{2\varepsilon ox}{\varepsilon si\ tsiteq}V^{'}Gsi$$

$$\rightarrow (33)$$

Solving second order differential Equation , we get

$\Psi si(x) = Cie^{p(x-xi-1)} + Bie^{-p(x-xi-1)} + Ki \rightarrow (34)$

here$p = _2\varepsilon ox/\varepsilon sitsiteq \rightarrow (35)$

$Ki = (VGSi - qNA/\varepsilon sip2)\ . \rightarrow (36)$

The coefficients A1, *B*1, *A*2, *B*2, *C*3, *B*3 can beexpressed as

$$A_1 = \frac{1}{2\sinh(px3)}\Big\{(Vbi2 + VDS - K3) - (Vbi1 - K1)e^{-px3} \rightarrow (37)$$

$$-(K1 - K2)\cosh(p(x3 - x1))$$

$$-(K2 - K3)\cosh(p(x3 - x2))$$

$$B_1 = \frac{1}{2\sinh(px3)}\Big\{(Vbi1 - K1)e^{-px3} - (Vbi2 + VDS - K3) \rightarrow (38)$$

$$+(K1 - K2)\cosh(p(x3 - x1))$$

$$+(K2 - K3)\cosh(p(x3 - x2))$$

$$A_2 = A_1 e^{px1} + \frac{K1 - K2}{2} \rightarrow (39)$$

$$B2 = B1\ e^{-px1} + \frac{K1 - K2}{2} \rightarrow (40)$$

2. Electric Field Distribution Model for TMDGTFEs

The electric field distribution in the channel is modified such that the field near the source becomes larger causing a more rapid acceleration of the electron .Thus the average carrier transport velocity in the channel is increased ,which leads the enhanced performance of the device.

The expression of electrostatic field can be written as

$$E_{xi}(x) = -\frac{\partial \varphi i\,(x,y)}{\partial x}\Big|_{y=0} \rightarrow (41)$$

$$= A_i\, pe^{p(x-xi-1)} - B_i pe^{-p(x-xi-1)}$$

$$E_{yi}(x) = \frac{-\partial \varphi i\,(x,y)}{\partial y} = Ci1(x) - 2yCi2(x) \rightarrow (42)$$

3.Drain Current Model for TMDG TFETs:

TheBTBT(band − to − band tunneling)Technique of charge carriers from its different regions determines the current flow of TFETs. The calculation of the drain current is based on Kane's model. The corresponding drain current derived from the following equation

$$I_D = q \int_{volume} \left\{ A_{Kane} Ex1(x) E_{avg}^{\gamma-1} \exp(-Bkane/Eavg) \right\} dv (43)$$

*L*min and *L*max are the initial tunneling length, longest tunneling length respectively. The distance from the junction of source-channel and the position where the surface potential of the device changes happens due to the unit bandgap potential amount is termed as the initial tunneling length

$$Lmin = (1/p)\ln\left(\frac{m+\sqrt{m2-4A1B1}}{2A1}\right) \rightarrow (44)$$

The term Lmax is represented as the variation in distance from the source –channel interface and highest surface potential position in the region of the channel

$$Lmax = ((1/2p)\ln\left(\frac{B1}{A1}\right)) \rightarrow (45)$$

we develop the equation of drain current (I_D) from the above equations

$$\left.\begin{aligned} &\frac{-A1}{P-\frac{B_{kane}\,q}{Eg}}(S1(Lmax) - S1(Lmin)) \rightarrow (46) \\ &I_D = I_O \frac{B1}{P+\frac{B_{kane}\,q}{Eg}}(S2(Lmax) - S2(Lmin)) \end{aligned}\right\}$$

$$Io = (qA_{Kane}E^{\gamma-1}\, p\, tsi\, /q^{\gamma-1}),$$

$$S1(x) = e^{\frac{\left(P-\frac{B_{kane}\,q}{Eg}\right)x}{x^{\gamma-1}}}$$

$$S2(x) = e^{-\left(P+\frac{B_{kane}\,q}{Eg}\right)x/x^{\gamma-1}}$$

4.Transconductance Model for TMDG TFETs:

The transconductance of the TMDG TFET can be obtained from the Drain current equation. The transconductance model equation can be written as

$$gm = (dID/dVGS)VDS = cons. \rightarrow (47)$$

$$= \frac{Io}{2\sinh(p(L1+L2))}\left\{ \begin{aligned} &\frac{(S1(Lmax)-S1(Lmin))}{(P+\frac{BKaneq}{Eg})}(1 - e^{-p(L1+L2)}) \\ &- \frac{(S2(Lmax)-S2(Lmin))}{(P+\frac{BKaneq}{Eg})}(1 - e^{p(L1+L2)}) \end{aligned} \right\}$$

3. Results And Discussion

SYMBOL	PARAMETER	VALUE
N_1	Source doping,cm^{-3}	$1*10^{20}$
N_4	Drain doping,cm^{-3}	$5*10^{18}$
$N_{3,}N_{4,}$	Channel doping,cm^{-3}	$1*10^{16}$
t_{si}	Silicon body thickness, nm	10
t_{ox}	Sio2 thickness, nm	1
t_k	High-K dielectric thickness ,nm	2
L	Channel Length, nm	50
$L1$	Tunneling Gate Length, nm	15
$L2$	Control Gate Length, nm	25
$L3$	Auxiliary Gate Length, nm	10
$\phi M1$	Tunneling gate work function,	4.2 eV
$\phi M2$	Control gate work function,	4.8 eV
$\phi M3$	Auxiliary gate work function,	4.0eV

Table.1 . The device model parameters

The device modeling parameters for Triple Material and duel material Double Gate TFETs are listed in Table 1.

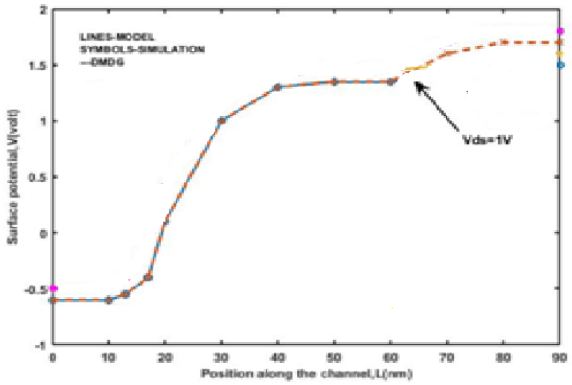

Fig 3(a). Surface potential of DM-DG TFET along the

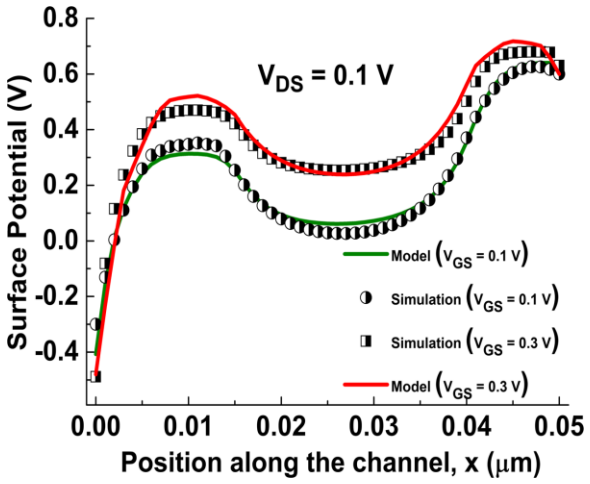

Fig.3 (b) Surface potential of TM-DG TFET along the channel for Vds

In Fig. 3(b). Surface Potential of Dual Material Double gate Tunnel FET is compared with the surface potential of DM-DG and TM-DG TFET. The results are plotted for channel length at x-axis and y-axis as surface potential. From the results it is observed that as per the nature of Triple Material we have the steep present which shows the variable work function. In this article, we used HfO2 material in place of a High-k dielectric constant. The surface potential of the device increases with an incrementation in gate-source voltage as additionally visually examined in TFETs. Figure 3 illustrates the surface potential of the device is varied for the various drain to source voltage (Vgs)along with the position of the channel. It shows the Drain induced barrier lowering is independent of the drain to source voltages. The effect of the drain-source voltages on the whole channel is diminutively minuscule, excluding the depletion regions.ergo, in the drain region of thedevice as a drain-source voltage(V_{ds}) increases the surface potential of the device furthermore increases for upper values of drain-source voltages(V_{ds}).The TCAD simulation results are shown the enhanced performance in Triple Material DG-TFETs when compared with Duel Material DG TFETs.

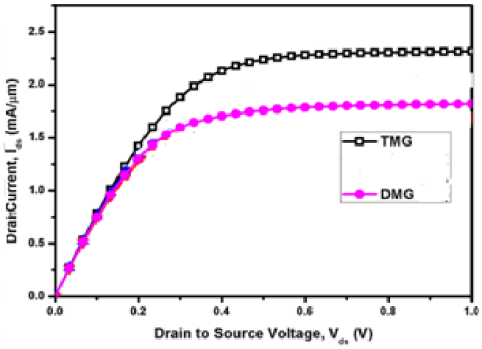

Fig 4. Drain current versus Drain-to-source voltage (Id vsVds)

In Fig.4.Drain current and Drain source voltage of DG-TFET is compared with I_d and Vgs of TM-DG TFET and DM-DG TFET. The results are plotted for drain-source voltage at x-axis and y-axis as Drain current. When there is an increase in drain current ,gate to source voltage increases. The Drain current increases due to more electrons enters from source to drain region and barrier height decreases with increasing Vgs . The TCAD simulation results are Shown the enhanced performance in Triple Material DG-TFETs when compared with Duel Material DG TFETs.

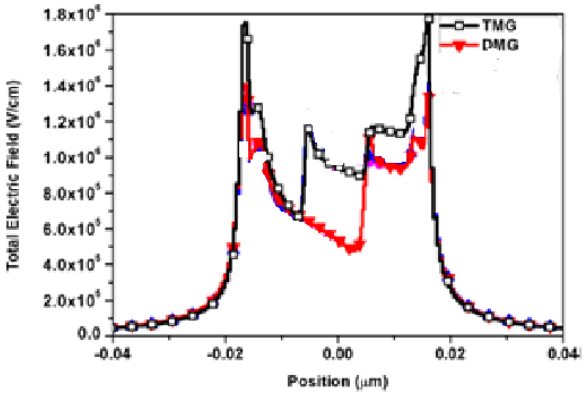

Fig. 5. Electric Field diagram of DMG-DG TFETs and TMG TFET

The graph shows the relation between the electric field and the position of the channel. The highest average electric field observed in the triple material DG TFETs, Which leads to higher ON current.

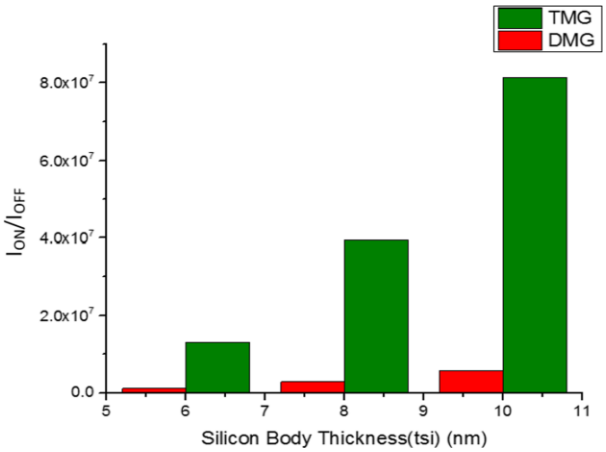

Fig. 6 Comparison graph of ION/IOFF ratio w.r.t. tsi

Figure 6 shows The ratio between ON- current and OFF-current (ION/IOFF) for the Triple Material-DG and Duel Material-DG TFETs. Due to the usage of Triple material, the value ION/IOFF is high when there is an increase in the thickness of silicon thickness when compared with the double TFETs

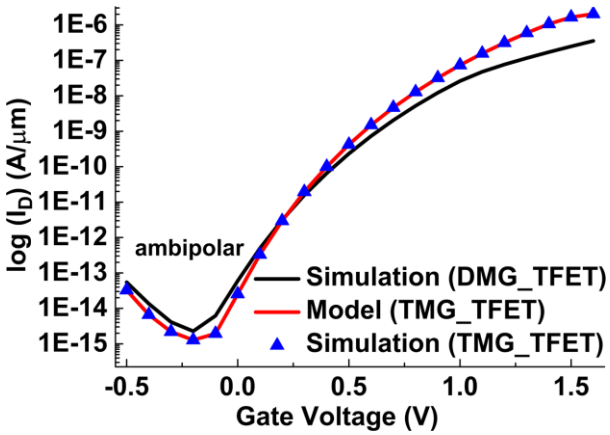

Fig. 7 Drain current vs. Gate source voltage for Triple Material-DG and Duel Material-DG TFETs

Figure 7 shows The variation of tunneling current and gate voltage for TMDG TFETs and DMDG TFETs .since, their improvement in dielectric constant, the gate takes a high level of control on the channel because the oxide thickness is getting reduced. This lead reduces the *L*min with the high values of dielectric constant. The decrease of *L*min shows the huge tunneling current through the junction between source and channel in Triple Material-DG when compared with Duel Material-DG TFETs is mentioned in the figure. The results are Shown the enhanced performance in Triple Material DG-TFETs when compared with Duel Material DG TFETs.

4. Conclusion

The comparison of DM-DG and TM-DG TFETs is done based on the characteristics such as surface potential, electric field, drain current, and the analytical model comparison based on 2D- Poisson's equation solved by parabolic approximation technique in the TCAD simulation environment. The results show the improved performance of the TM-DG TFETs based on the above characteristics when compared with the DMDG TFETs. The optimized *L*1, *L*2, and *L*3 of TM-DG TFET structure lead to attaining the upper bound of *ION/IOFF* ratio and lower Sub threshold Swing (SS) and ambipolar transport effects.

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