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CERTAIN PERFORMANCE INVESTIGATIONS OF VARIOUS PULSE TRIGGERED FLIP FLOPS

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***Abstracts*:** We know that power consumption has become major concern in the digital low power integrated circuit design over certain years. The power dissipation was a major problem in an integrated circuit design fabrication technologies which allows the use of nano-scaled devices. In many sequential logic circuits the flip flops are widely used in VLSI chips, without degrading other characteristics. In such cases the power consumption of those circuits should be improved. The power consumption of the clock tree system has been lowered by the simple circuit in the P-FF. It consists of strobe signal for pulse generation and data storage for a latch. The latches operate like an edge trigger flip flops. For high speed the triggering pulse are narrow for in P-FF and it gives the higher toggle rate. This paper is an attempt to review various pulse triggered flips flop design.

I. Introduction

In general a storage element (flip flop or latch) has two stable states and it is used for store state information. The distinction between two element (such as FF and latches) is that for latches are providing the enable signal is state information of the output (i.e.) in latches input changes the content of output changes immediately when they are in enabled state.

Flip flop are basic building block of integrated circuit used in computers, communication devices, memory systems etc . FF is used for store the states information (0 or 1) by counting pulses in infinite storage element. The output and the current input do not depended upon next state, but also on current state. The clock system contain clock sharing network and storage element, it is consumes more than 50% of the total system power. In a flip flop the state changes at the rising edge and also at the falling edge of enable signal (i.e.) the clock signal. The widely used existing processor designs are Master slave flip flop, sense amplifier based flip flop and pulse triggered flip flop which is constructed with master and slave which are categorized by their property of hard edge triggering.

The pulse trigger flip-flop has characterized by two stages to reducing their larger delay. Therefore to reducing delay between output and input the soft edge property and a negative setup time is used in pulse generator. The categories of P-FF is Ip-FF and Ep-FF are one of categories in P-FF[2]. The static or semi-static dynamic or semi dynamic logic can be applicable in P-FF. In the Ip-FF[2] the pulses generated inside of the FF such that (HDFF) hybrid latch FF, (SDFF) semi dynamic FF, (Ip-DCO) [1] implicit-pulse data close to output FF are example of Ip-FF. The pulse are generated externally in (Ep-DCO) [1] explicit-pulse data close to output FF it is the example of explicit pulse triggered flip flop.

II. Literature Survey

Jin Fa Lin et al.[1] has designed CMOS low power flip flop based external type and modified design of true single phase clock latch. The author has discussed some existing P-FF such as Ep-DCO, CDFF, static-CDFF, MHLFF [1]. The main drawback of this flip flop is long discharge path problem and larger switching power, longer delay dissipation [1].

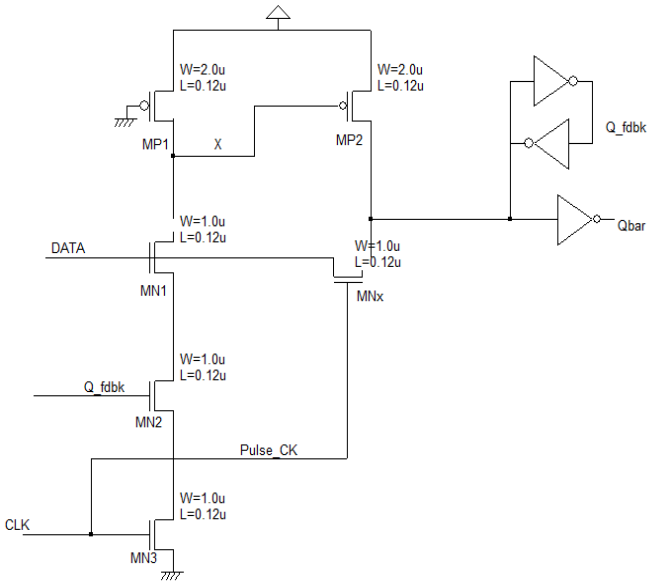

Fig.1. Schematic design P-FF design.

The Fig.1 shown in P-FF design[1], the signal feed through technique is used to avoid the switching activities in the internal nodes this scheme employs to reduce the delay also. In this design applicable to static latch structure method and conditional discharge method. In this P-FF [1] design transistor MP1 is a feeble pull-up PMOS transistor it gives rise to a pseudo-NMOS logic structure design. Second MNx pass transistor controlled by clock signal which is contain the input data it can force the latch 'Q'node directly. The extra driving to Q node at '0' to '1'transition and '1' to '0' transition at discharge node is provide by transistor MNx.

The operations of the above design (Fig.1) as follows. The clock pulse is given, the input data and node 'Q' are maintain at same state, the transistor MNx becomes the input stage signal switching, it can occurs in any of the internal nodes. The "0" to "1", data change occurs a node X is discharged the transistor MP2 comes to on state, which is triggers the node Q to high. To referring Fig.1, the FF operations as the discharging path conducts only for a clock pulse duration which is gives the worst case timing sequences. On the other hand, the MNx pass transistor input and the delay can be greatly reduced. Pass transistor MNx is similarly turned on through clock pulse and node 'Q' is discharged through input stage by this route in case of data transition "1" to "0". Unlike the input source allows the discharging the data transition '0' to '1',. In view of that MNx is turned on at short time slot, the loading effect is not significant at

input source. The critical path delay and modification of transistor size to improve the speed this improvisation is does not related to discharging effect.

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Saranya. L et al [2] has designed the three categories of conventional triggered FF for the low power pulse-triggered flip-flop methods such as ip-DCO(implicit pulsed data-close to output),MHLFF, SCCER and their design conceded in the best power delay performance.[2]

The Ip-flip flop the pulse is generated inside only, DCO means that output is kept closer to the input node which gives lesser delay to output node. The complexity of the locking mechanism in hybrid latch FF reduces the small delay and area. In modified version of hybrid latch flip flop has minimum number of transistors and also less power consumption. In SCCER circuit an AC type supply voltage is used which has minimum energy dissipation and it is restricting current flow across the circuit with low voltage drop and the capacitor stores the recycling energy.

The design of MHLFF shown in Fig.2, it's compared with HLFF the MHLFF internal node transition occurs only when the input has different logic values at two successive clocks. The node 'X' is low level or remains charged to 'V_{dd}' which is depends upon the state of input. At rising edge node the "D" has high transition logic value the 'X' is discharged through transistor N_1 and N_3. Therefore Q is charged equal to Vdd and residue to high at clock period. The transistor P_1 will be OFF state. If D has high value in the next rising edge of the clock, in different to previous logic, there is no changeover in X, which is pass up the extra power utilization. To evaluate the HLFF, the state of flip-flop is used to remain the state of internal node in anticipation of input condition is changed. The number of transistors in the design configuration is less than that of HLFF, so the MHLFF is faster than HLFF. The lower power utilization of MHLFF with enhancement in delay and area compare to others logic. When data is '0' and clock pulse is '0', P_2 transistor force to ON and it passes the complement value of clock that is '0' to '1' the transistor N_3 is turned ON that passes the value '0' to the above stage.

The transistor N_1 is OFF since the data is stay at "0", while the transistor P_1 is turned OFF for this reason node X will be remain "1". The output N_2 transistor '0'when is comes to ON state. When clock pulse is '0' and data is '1', P_2 transistor will comes to ON state and it passes the clocks complement value that is '1' to transistor N_3 which is turned ON the value '0' to the above stage. Since the data is remain '0' N_1 transistor is remains at ON state where as the transistor P_1 is turned OFF hence the node X will be '0' and the transistor N_2 is ON the output is 1. By using larger transistors of N_3 and N_4 of this design the redundant switching problems to enhance the discharging of power capability can be eliminated. An additional design problem is

that input Data and output Q both equal to '1' the node turn out to be floating. Further adding a DC power it emerges if node X is floated from an integral '1'.

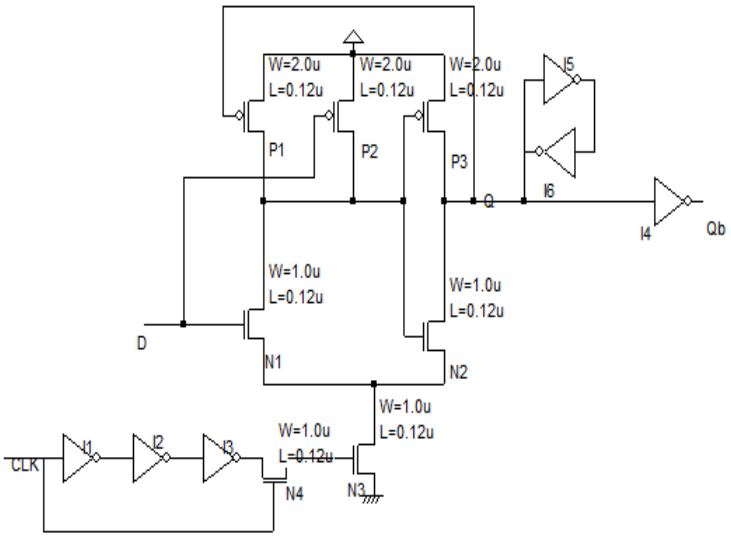


Fig.2. Hybrid Latch Flip-Flop

Tania Gupta et al.[3], has compared three existing design of dual edge triggered FF such as E_P-CDFF, ED-CPFF and DET-SAFF. The pulse generator and conditional discharge have been included in EP-CDFF [3] which is produces the active dual pulse at both rising edge and falling edge clock pulse. In EP-CPFF the condition precharged technique is used for removing the redundant transition it cause for decrease the power dissipation. The sense amplifier used in DET-SAFF [3] design to removes the unnecessary changes in internal nodes when current data is in ideal for long time and significantly disable the clock, when the input which supports no output changes in a control circuitry.

In the latch part the power reduction technique is applied when the input is in identical state for the extensive time period which is not adequate. In the author proposed a few controlling circuit which is disabling the clock, when the input invokes no output. The data dependent technique based flip-flop is proposed to reduce the unnecessary transition. The clock is disabled at the point when no significant state changes at output because of stable input it saves utilization of power.

The "XOR" operation is made between 'D' and 'Q', and 'D_B' and 'Q_B' as shown that is depends upon the data because basically it has compares the data 'D' with the output 'Q'. Then the control signal 'GCLK' is gives the pulse to generator and then sensing stage in which logic amplifier is used and after that latch part is used. The schematic flip-flop is shown in Fig.3.[3]

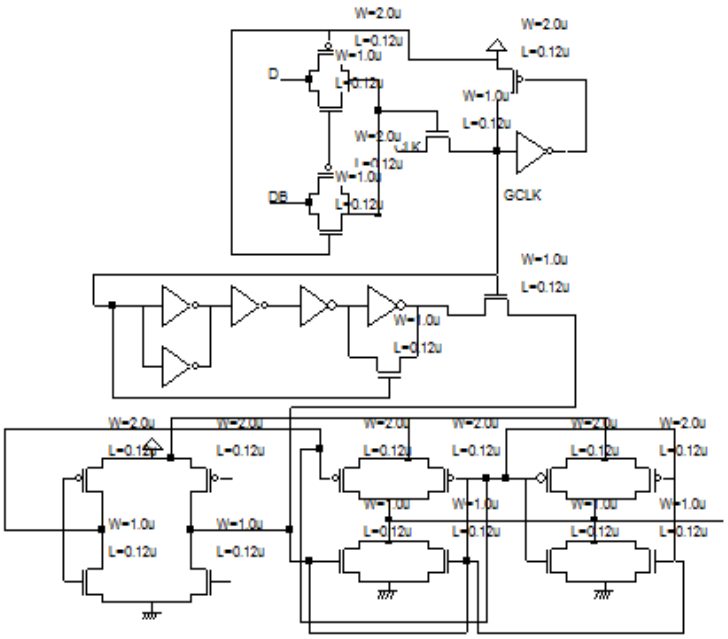


Fig.3. Schematic of EP_CDFF

Massimo Alioto et al. [4][5] has designed a logic and compared 19 different designs belonging to four different classes in CMOS 65-nm technology. The comparison parameter are considered the layout parasitic leakage capacitance in both standby mode and active mode wide load and switching activity. In the above analysis the short listed the fastest topology i.e., STFF. The best low power and energy FFs are DETTGLM [4] and TGFF [4], where as more energy efficient s TGPL. The design STFF (Skew Tolerant Flip-Flop) shown in fig.4.(a), it is has constructed in two stages. The Stage one produces a pulse at node S/ S' (Set) or R/R' (Reset) after the falling edge of Clk. The stage two is a set-reset latch that detain the pulses S/S' or R/R'. at high clock pulse the node CS and CR are low transition. The Node S' and R' changes to high transition the I_3, I_4, M_{10}, M_{12}, M_{14} and M_{16} maintain the values of outputs Q and Q' value. When clock switches to low signal CS and CR are driven to high and to enabling evaluation of nodes S'

and R'. If D=1 (D=0), node S'(R') switches low and node S (R) high, which forces CR (CS) reverse to low transition. This disables subsequent switching of node R'(S') and ensures that node CS(CR) is driven high while Clk=0. The pulses at S/S' or R /R' simultaneously pull Q/Q' to D/D'. During the time when Clk=0, the low level of node S' (R') is retained by transistor M_1 and M_3 (M_5 and M_7).

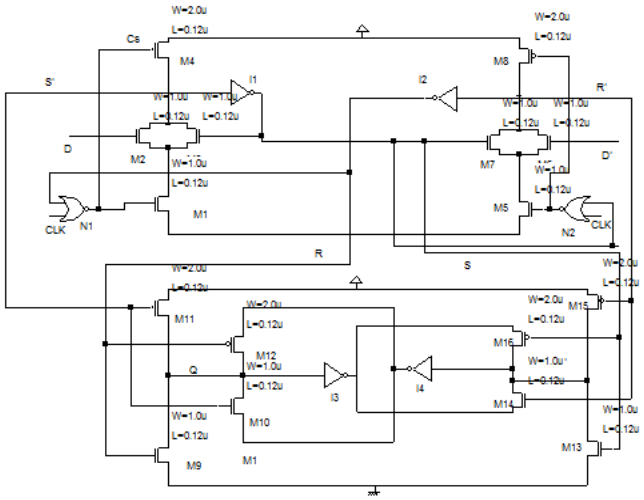


Fig.4.(a) Schematic of STFF

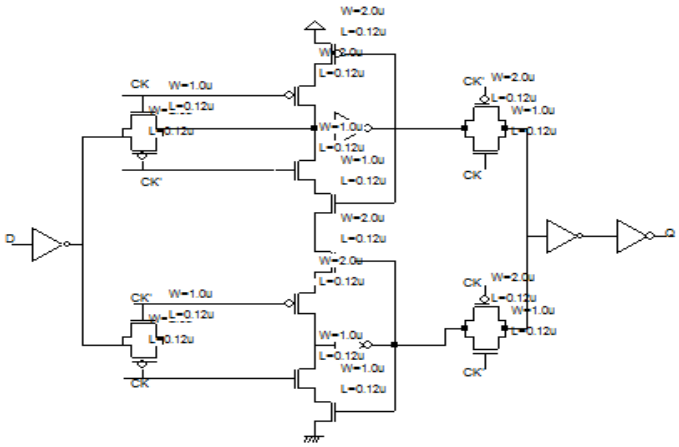


Fig. 4.(b). Schematic of DET-TGLM

A DET flip-flop [4] Fig.4.(b), modifies its output at every clock edge. As a result, the of the clock frequency can be share equally while it comes the same data throughput its lead to a significant drops in power dissipation.

The TGFF with input gate separation is obtaining from the pair of power latch, where the input gate separation is gives the better noise resistance. An inverter circuit provides non-inverting output in TGFF. The TGFF, is the fastest classical logic structures. The main advantage classical logic structures is the short direct path and the low feedback power. The clock will greatly affect the total power consumption of the flip-flop because of the large load. The TGFF has fully static master-slave design, which is structured by cascading two identical pass gate latches and it has give a short clock to output latency. The positive setup time creates the poor data to output latency. In additionally, it has sensitive to clock signal slope and data feed through. To reduce the clock load we have minimize clocked capacitances in order. The transistor size optimization method is used in this logical effort. The off-path capacitance is equal to the gate capacitance of two minimum width of feedback transistors. The keeper circuit in the feedback of latches are have minimal width. The little impact on the setup time and minimum sizing of the master stage takes minimum the energy consumption. In author investigate, the benchmark TGFF with internal clock gating. Figure 4. (c).

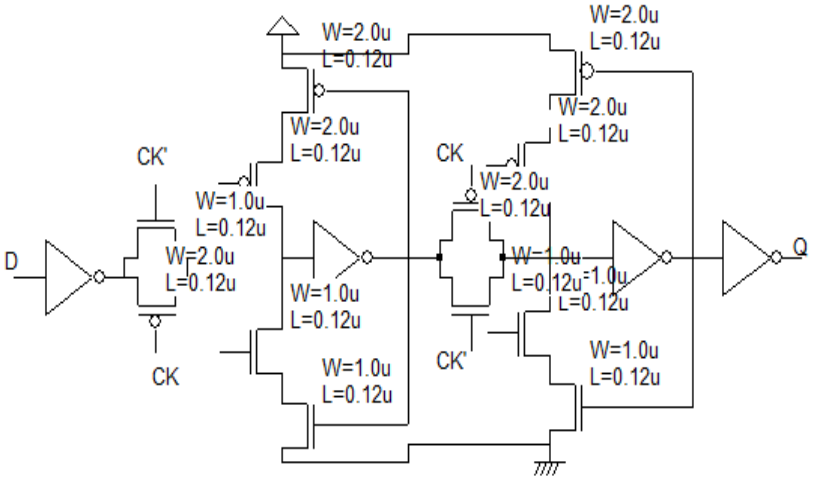
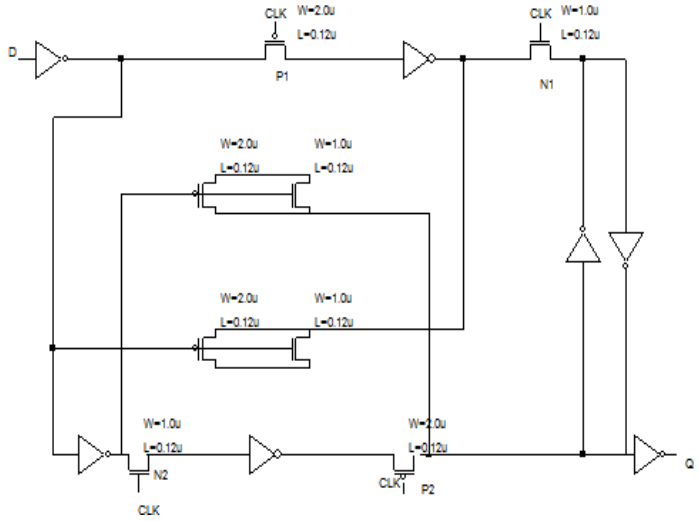


Fig.4.(c) Schematic of TGFF

Chen kong et al. [4] have examined adaptive-coupling flip flop design with use of D-FF which has reduced the number of transistor and as compared to other flip-flops (TGFF) using CMOS 40-nm technology. A new method, the adaptive-coupling scheme shown in Fig. 5, the input state is different to its internal state it creates weak state-retentions coupling in ACFF . This sequence enables a easy transition, and allows ACFF to have a good process variations. An ACE (adaptive-coupling element) is containing of a PMOS and a NMOS, constructed in parallel, and the data signal controls all the gates. Consider the ACFF Fig.5 If the gate level is high which means BN node is high, B node is low, the PMOS is goes to off state and the NMOS is comes to on state, it creates the charging ability between G to F path which is enables the state of node F to be easily lowered to VDD-V_t, for the duration of discharging through the F-B path. Since a PMOS between the F-B path, the node F cannot be completely discharged. When node G turns into a low state by charging of node FN, node F is completely discharged to 0V through the F-G path, since the ACFF NMOS allows a strong discharge current.



. Fig. 5. Schematic of Adaptive-Coupling Flip-Flop (ACFF)

ACFF s more energy efficient than TGFF uses a single phase clocking structure with no load and pre-charging stage it saves upto 77% of energy. It has minimum standard deviation of delay times especially at 0.8V with 18ps as compared to 34ps for TGFF. ACFF design replaces about 84% of the FFs it is having a larger setup time than TGFF

Massimo Alito et al.[7][8], has examined a variety of flip flop to checks the clock slope on the speed and overall power dissipation of both FFs and clock buffers using CMOS 65-nm technology have been analyzed by author fig 4.(a),(b),(c). Their result showed that 30% to 40% energy saving with minimum the clock slope it can be relaxed with custom assumptions, and they discussed in terms of additive clock skew and clock jitter properties in clock slope for the existing classes of FFs. The analysis of energy contribution FFs energy increases through the smoother clock slope and energy dissipated decreases by the local clock buffer has been in clock domain circuit. The FFs energy dissipation is more seriously deal with speed of FFs which is unchanged by clock slope has been exposed through their analysis.[7],[8]

Dai Yan-Yun et al.[9] flip flop design based on transmission voltage switch theory in CMOS 0.18μm technology, this method is suitable for all kinds of P-FF and not need any further work for reducing the switching activities of internal nodes. In proposed structure two pulsed flip flop (D and JK flip flip) were executed. The D-FF has 17.2% of delay and 30.1% power delay products in author analysis.[9]

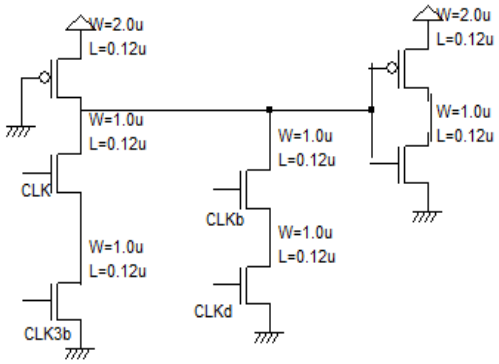
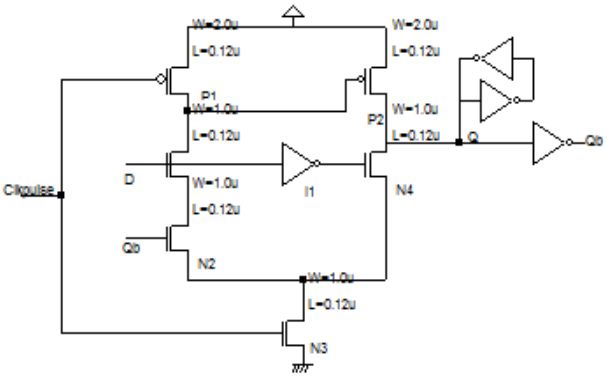


Fig. 6.Schematic of D flip-flop: (a) Pulse generator;

The D flip-flop shown in Fig.6,[9] the simulated in advanced Ep-DFF, which is a dual-edge trigger explicit-pulse dynamic D flip-flop (named as CDFF) and presented in the simulation condition of the proposed D flip-flop. Above designs are compared in the property of delay, total power and power-delay product. The difference between input and output is measured as the delay time of the FF, which contain both setup time and clock to output (CLK-to-Q) delay. The power utilization of the flip flop includes the internal power dissipation, local clock power and local data power dissipation. The internal power dissipation of the flip-flops increases due to output capacitance switching it has eliminates to get the reduced net internal power dissipation.

Peiyi Zhao et al.[10], proposed a technique called as clustered voltage scaling(CVS) using in conversion flip flop(CPN-LCFF). To decrease power dissipation and without disturbing the circuit performance efficient way has been followed . The CVS uses speed insensitive paths in low and high supply voltage is speed perceptive path it reduce the system power utilization.



(b)

Fig.6. Schematic of D flip-flop (b) Pulsed latch

The various level shifting flip flop topologies shown in Fig.7,[10] differential style, NMOS PT style, and CPN-LCFF) technique. The CPN-LCFF generate in terms of power and delay by 8% and 15.6% and overcomes the previous LCFF respectively. It is suitable for low power high performance systems. The NMOS-CPN level-shifting scheme is proposed Fig 7.(a). In this scheme, the PMOS is always ON. The conditional discharge technique[6] the feedback signal controls NMOS. When input stays high, will shut off to avoid redundant short-circuit current as well as the redundant switching activity at the node. Low-swing signals including input signal and a clock pulse are connected to the NMOS[12],[14] device. A LCFF AND CPN_LCFF is proposed. It is connected to transistor N_5 is used to disconnect discharge path when Q=1 and Q_FB=0 the second NMOS branch is responsible for pulling down the output.

The CP-NMOS scheme is different from the general idea of conventional pseudo-NMOS logic in this design the clocked transistors in the pull-down branch as well as a conditional discharge feedback is used to control transistor. To comparing this with previous level-shifting, the proposed level-shifting technique employs only single PMOS, the resulting design well efficient design. One thing to be noted that it might be need more hold time for pulsed flip-flops than conventional flip-flops.

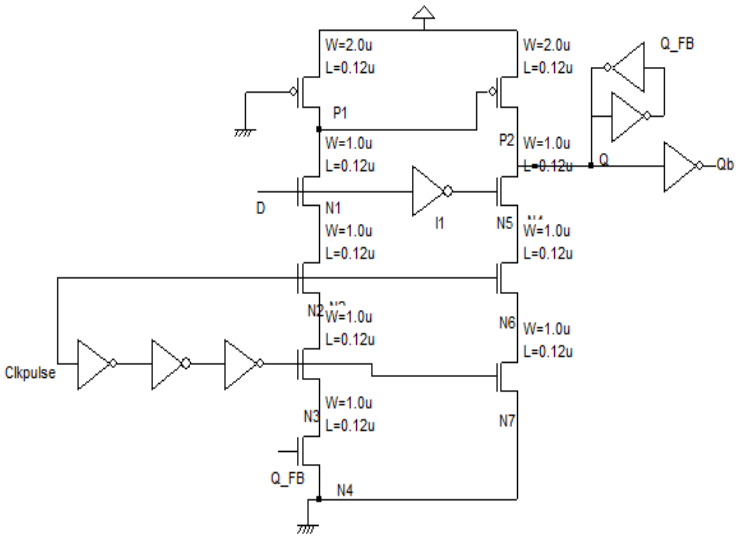


Fig.7. Schematic of CPN-LCFF

III. Gated JK FF design

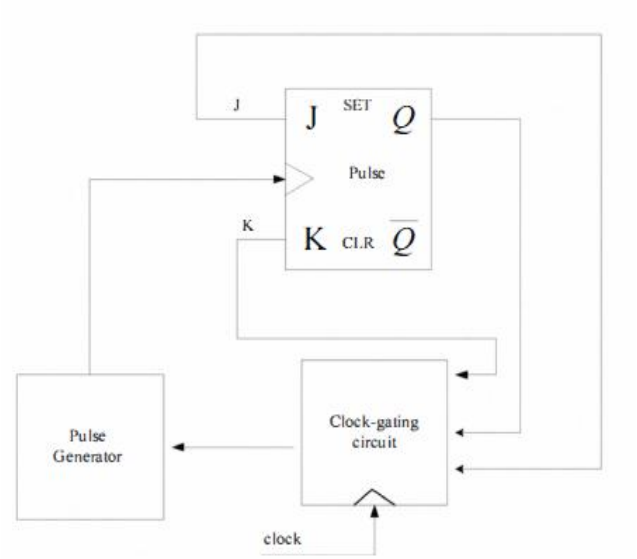


Fig. 8.proposed block diagram of the design

In this method CG-PT-DET is used[11] . The whole design is shown as fig.8. In this the author Xianghong *etal* has proposed technique, for the improvements in pulse generator circuit and utilize clock-gating technique to make it more power-efficient.

In the pulse generator to eliminate the redundant transitions, the clock-gating pulse generator is constructed. It utilizes the DET-SAFF design is based on and incorporates the clock gating technique. In this circuit, the author Xianghong *etal.* has used clock gating technique by embedding a control circuit in the explicit pulse generator in this method pulse signal generator is masked in a redundant event which mean it comes to a sleep mode. The considered schematic diagrams of the clock gated pulse generator are shown in Fig.9. For example, when the next state of the flip-flop is the same as before, X signal will be low and CN_3 will be closed, so the clock won't pass CN_3, and CLK_1 will be masked and will be having zero value, as a result, the JK flip-flop will keep the state and since the CLK is not been applied the power consumption will be much less , on the contrary, when the state toggles in the flip-flop is different from before, X signal will be high and the pulse generator will produce a pulse, the flip-flop will change its state as its logic function. Figure 9

The simulations illustrate that the power consumption reduces apparently when the activities of the JK flip-flop are lower than 40%. For in this condition, clock-gating technology

applied in this circuit cuts off all the unnecessary transitions, at 60% of the time, most of the circuit are difficult and hardly consume power.

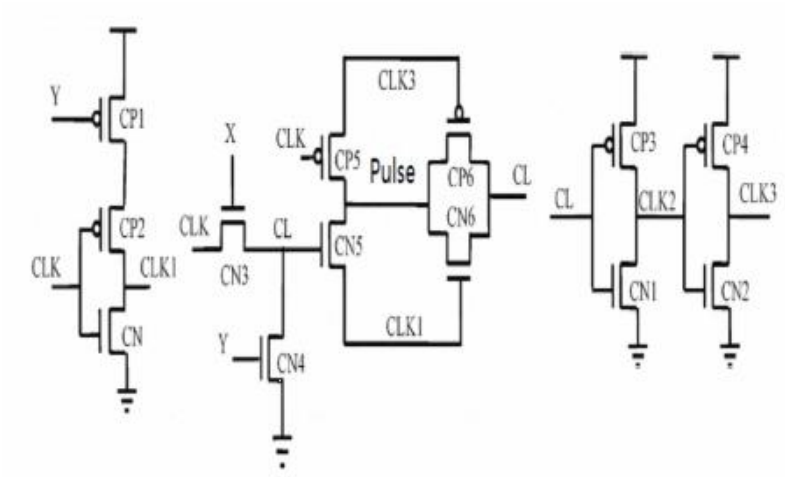


Fig. 9.Clock-gating pulse generator

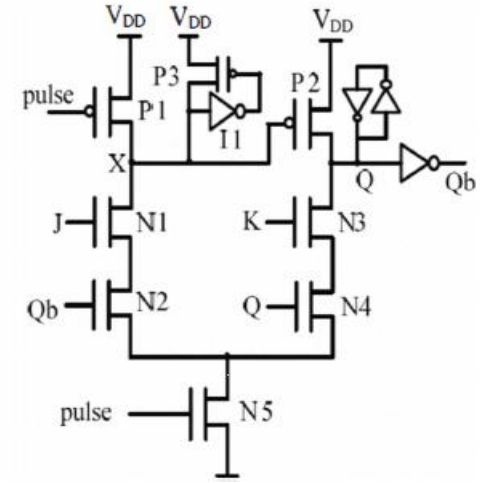


Fig. 10.Proposed JK flip-flop design (CG-PT-DET)

IV. Experimental Discussion

In this study, flip flop are categorized into various triggering method based upon their clocking ability and topology. The pulse triggered flip flop were only examines based on the

power dissipation. Moreover each design are concentrated on the clocking strategies[15],[16],[17],[18] which is based on signal feed through scheme, single edge triggering and dual edge triggering methods. The impact of the above review provides the data that the clocking circuit is consuming more dynamic power in the flip flops. For low power clocking system various CMOS[13] circuit designs methodologies are reviewed. This survey presents the significance and drawbacks of several pulse triggering flip flop circuits along with comparison of proposed circuit.

The types of FF designs using variety of transistors and their simulations results pertaining power and delay studied through detailed survey are provided in table 1.

FF Designs	Ep-CDFF	MHL FF	CDFF	TGFF	STFF	ACFF	P-FF	proposed
Number of transistors	30	19	24	22	25	22	24	21
Layout area (μm2)	89.70	78.94	72.20	88.13	66.96	84.87	69.13	65.44
Setup time (ps)	−88.2	1.5	−73.2	67.3	−26	112	−85.7	1.22
Hold time (ps)	123.5	95.7	137.1	−45.3	55.3	−60.9	120.1	83.7
Minimum D-to-Q delay (ps)	129.5	173.8	136.8	271.4	132.5	284.5	109.1	126.2

Table.1. Comparison of Various FF Designs

3. Conclusion

In this brief, various triggering methods are available but they are seemed to consume more power in clocking circuit due to common clocking throughout the design in my proposed work a novel CG-PT-DET design is simulated using tanner EDA tool by employs clock gating structured latch. In that structure incorporate with various mixed design style consisting clock gating pulse generator JK flip flop[11]. This key idea is to reduce the dynamic power utilization[23],[24] in the flip flop circuit, which would be facilitate the extra clocking power to shorten the clock utilization to enhance the area, power and speed performance.

REFERENCES

[1] Jin-Fa Lin, "Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through Scheme," IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 22, No. 1, January 2014.

[2] Saranya. L, Prof. S. Arumugam, "Optimization Of Power For Sequential Elements In Pulse Triggered Flip-Flop Using Low Power Topologies," International Journal Of Scientific & Technology Research Volume 2, Issue 3, March 2013.

[3] Tania Gupta, Rajesh Mehra, "Efficient Explicit Pulsed Double Edge Triggered Flip-Flop by Using Dependency on Data," IOSR Journal of Electronics and Communication Engineering (IOSRJECE), Volume 2, Issue 1 (July-Aug 2012), PP 01-07.

[4] K. Chen, "A 77% energy saving 22-transistor single phase clocking D-flip-flop with Adoptive - coupling configuration in 40 nm CMOS," in Proc. IEEE Int. Solid-State Circuits Conf., Nov. 2011, pp. 338–339.

[5] M. Alioto, E. Consoli and G. Palumbo, "Analysis and comparison in the energy-delay-area domain of nanometer CMOS flip-flops: Part II - results and figures of merit," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 5, pp. 737–750, May 2011.

[6] P. Zhao, T. Darwish, and M. Bayoumi, "High-performance and low power conditional discharge flip-flop," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 5, pp. 477–484, May 2004.

[7] M. Alioto, E. Consoli, and G. Palumbo, "General strategies to design nanometer flip-flops in the energy-delay space," IEEE Trans. Circuits Syst., vol. 57, no. 7, pp. 1583–1596, Jul. 2010.

[8] M. Alioto, E. Consoli, and G. Palumbo, "Flip-flop energy/performance versus Clock Slope and impact on the clock network design," IEEE Trans. Circuits Syst., vol. 57, no. 6, pp. 1273–1286, Jun. 2010.

[9] DAI Yan-yun, SHEN Ji-zhong, "Structure and design method for pulse-triggered flip-flops at switch level," Springer 2010.

[10] P. Zhao, J. McNeely, S. Venigalla, G. P. Kumar, M. Bayoumi, N. Wang, and L. Downey, "Clocked-pseudo-NMOS flip-flops for level conversion in dual supply systems," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 9, pp. 1196–1202, Sep. 2009.

[11] Xianghong, Zhao, Guo Jiankang, and Song Guanghui. "An improved low-power clock-gating pulse-triggered JK flip-flop." Information Networking and Automation (ICINA), 2010 International Conference on. Vol. 2. IEEE, 2010.

[12] Easwaran, M. "Electrical dark soliton generation using CMOS seven stage ring oscillator with adaptive bias control", Journal of Advanced Research in Dynamical and Control Systems, vol. 9, pp. 978-984, 2017.

[13] Easwaran, M., and R. Ganapathy. "DARK SOLITON GENERATION USING CMOS RING OSCILLATOR.", ARPN Journal of Engineering and Applied Sciences, vol. 13, no. 3, pp. 852-858, Feb 2018.

[14] Easwaran, M,. "Dark soliton generation using N-Channel MOSFET.", International Journal of Pure and Applied Mathematics, vol. 117, pp. 667-673, 2017.

[15] H. Mahmoodi, V. Tirumalashetty, M. Cooke, and K. Roy, "Ultra low power clocking scheme using energy recovery and clock gating," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 1, pp. 33–44, Jan. 2009.

[16] S. H. Rasouli, A. Khademzadeh, A. Afzali-Kusha, and M. Nourani, "Low power single- and double-edge-triggered flip-flops for high speed applications," IEE Proc. Circuits Devices Syst., vol. 152, no. 2, pp. 118–122, Apr. 2005.

[17] M.-W. Phyu, W.-L. Goh, and K.-S. Yeo, "A low-power static dual edge triggered flip-flop using an output-controlled discharge configuration," in Proc. IEEE Int. Symp. Circuits Syst., May 2005, pp. 2429–2432.

[18] Nikola Nedovic, Marko Aleksic, Vojin G. Oklobdzija, "Conditional Pre-Charge Techniques for Power-Efficient Dual Edge Clocking," ISLPED'O2, August 12-14, 2002.

[19] V. G. Oklobdzija, "Clocking and clocked storage elements in a multi gigahertz environment," IBM J. Res. Devel., vol. 47, no. 5, pp. 567–584, Sep. 2003.

[20] Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, "Comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high-performance microprocessors," in Proc. ISPLED, 2001, pp. 207–212.

[21] B. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statistical power reduction," IEEE J. Solid-State Circuits, vol. 36, no. 8, pp. 1263–1271, Aug. 2001.

[22] A. P. Chandrakasan, S. Sheng, and R W. Brodersen, "Low-Power CMOS Digital Design," IEEE Journal of Solid-State Circuits, vol. 27, no. 4, pp. 473-484, April 1992.

[23] P. Zhao, J. McNeely, W. Kuang, N. Wang, and Z. Wang, "Design of sequential elements for low power clocking system," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 5, pp. 914- 918, May 2011.

[24] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, "Comparative Delay and Energy of Single Edge-Triggered & Dual Edge-Triggered Pulsed Flip-Flops for High-Performance Microprocessors,"ISLPED'01, pp. 147-152, Aug. 2001.