Device Engineering of Dual Metal Gate-Based Artificial Synapse for Enhanced Plasticity Utilizing Al_2O_3-Based Ion Conducting Electrolyte

Reetwik Bhadra, Ramesh Kumar, and Amitesh Kumar, *Member, IEEE*

***Abstract*— An energy-efficient artificial neuron can be developed with synaptic transistors using the electric double-layer (EDL) effect in the transistor's oxide layer. This work proposes a dual metal gate (DMG) engineered indium-gallium-zinc-oxide (IGZO) transistor utilizing a novel Al_2O_3-based ion conducting electrolyte for tunable synaptic performance based on the ion drift-diffusion model. The simulation has been carried out at an ultralow voltage of 0.5 V employing two connection schemes. The results show accurate simulations of synaptic activities like paired-pulse facilitation, excitatory postsynaptic current (EPSC), memory transition from short-term to long-term, depression, and dynamic filtering characteristics. To validate the device's performance, voltage, frequency, and pulse interval modulation have been carried out to determine the synaptic strength of the device. The dual metal assists in a higher ON/OFF ratio, leading to more robust potentiation and depression characteristics. The results imply that the DMG-based EDL device proposed provides a physical understanding and helps to relate the artificial synaptic transistors with a biological neuron.**

***Index Terms*— Dual metal gate (DMG), electric-double-layer (EDL), indium gallium zinc oxide (IGZO), synaptic transistor.**

I. Introduction

THE human brain can be mimicked by a highly efficient artificial neuron. The low power consumption of such devices and the capability of parallel information processing have made them superior to the conventional Von Neumann architecture [1], [2]. Learning and memory are fundamentally based on synaptic plasticity [3], [4]. As a result, it is crucial to emulate human brain computation through artificial synapses when creating neuromorphic systems [5], [6].

Various research has been carried out recently to simulate indium gallium zinc oxide (IGZO)-based neuromorphic devices to familiarize with the human brain [7], [8]. Electric-double-layer (EDL)-based devices that use inorganic dielectrics as an ion-conducting medium and insulating material have been under observation recently [9]. The EDL formation at the interfaces of semiconductor and gate leads to high specific capacitance and high charge density, thereby enabling low voltage operation [10], [11]. Synaptic devices based on EDLTs typically show very low power consumption because of the intense EDL modulation effect [12]. The synaptic weight regulation in biosystems, where data are transferred through ionic fluxes, is comparable to the ion-related electrostatic modulation in the EDL device [13]. IGZO-based TFT transistors are widely used because of their high efficiency and excellent electron transport properties [14], [15]. Additionally, solution-processed IGZO effectively lowers its preparation and processing costs [16]. Synaptic transistors with LTD or short-term plasticity (STP) behavior were reported recently, but not simultaneously [17], [18]. Recent research has focused on comprehending the relationship between synaptic plasticity and neurological conditions to potentially reduce symptoms or delay the course of specific neurological and mental disorders [19], [20]. IGZO-based synaptic transistors have found extensive application, especially in fields like pattern recognition and neuromorphic computing [21], [22]. Various synaptic transistors using electrolytes have been proposed to date [23]. With scalability at its peak, to suppress the rise in gate leakage at the oxide-silicon interface Al_2O_3 is preferred over SiO_2 [24]. A high-K dielectric material would cause a higher current to flow through the device, increasing its energy consumption [25]. Memory design employing Al_2O_3 as the ion-conducting electrolyte medium along with dual metal gate (DMG) is proposed for the first time. The effect of DMG in strengthening potentiation and depression has been carefully studied from the characteristics of the proposed device using the drain current regulation technique.

In this article, a DMG-based electrically modulated EDL device with an IGZO channel and Al_2O_3-based ion conducting

Manuscript received 16 January 2024; accepted 14 February 2024. Date of publication 26 February 2024; date of current version 26 March 2024. This work was supported by the Department of Science and Technology (DST), Government of India has aided the work under Department of Science and Technology (DST) Science and Engineering Research Board (SERB) Project, under Grant SRG/2021/002110. The review of this article was arranged by Editor T.-H. Kim. *(Corresponding author: Amitesh Kumar.)*

Reetwik Bhadra is with the Nextgen Adaptive Systems Group, Department of Electrical Engineering, and the Department of Electrical and Engineering, National Institute of Technology Patna, Patna 800005, India (e-mail: reetwikb.ph21.ee@nitp.ac.in).

Ramesh Kumar is with Department of Electrical and Engineering, National Institute of Technology Patna, Patna 800005, India.

Amitesh Kumar is with the Nextgen Adaptive Systems Group, Department of Electrical Engineering, National Institute of Technology Patna, Patna 800005, India (e-mail: amitesh.ee@nitp.ac.in).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2024.3367663.

Digital Object Identifier 10.1109/TED.2024.3367663

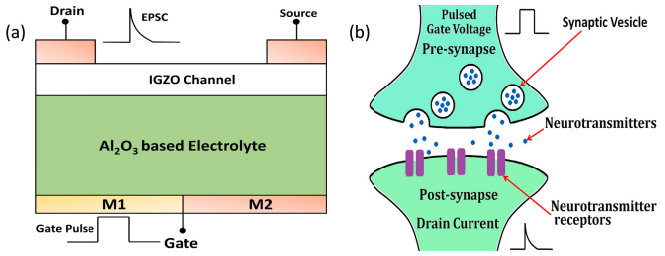

Fig. 1. (a) Schematic diagram of the IGZO-based synaptic device. (b) Biological synaptic neuron.

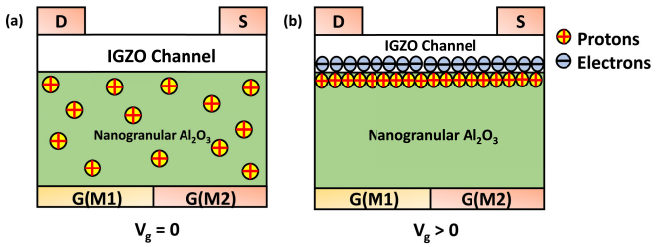

Fig. 2. (a) Proton distribution in the Al_2O_3 electrolyte film in the absence of gate voltage. (b) Protons accumulate at the Al_2O_3/IGZO interface on the application of a positive gate voltage, creating an EDL.

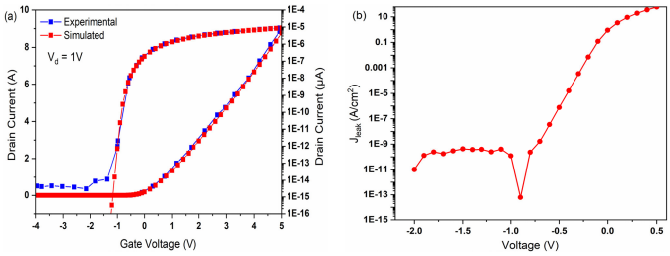

Fig. 3. (a) Comparison of simulated transfer characteristics with experimental data [26]. (b) Gate leakage characteristics.

electrolyte is modelled and simulated as a neuromorphic device. The simulated device demonstrates both temporary and permanent synaptic plasticity. Pulsewidth modulation at different frequencies has helped in successfully realizing the tunable synaptic behavior in the device. Besides, it is essential to study all the synaptic functionalities on a single device. Device modelling is therefore critically needed in EDL devices that exhibit the entire synaptic spiking behavior.

II. Device Specifications

As shown in Fig. 1(a), the schematic of the device with a DMG, Al_2O_3-based ion conducting electrolyte and an IGZO the channel is presented. Fig. 1(b) portrays a typical biological synapse in a human brain. The IGZO channel is 1 μm in length and has a thickness of 15 nm. The various parameters indicating the semiconductor properties of the electron and holes in the a-IGZO channel have been adjusted as necessary to carry out the fitting process while maintaining consistency with the [26].

The channel's electron affinity is kept at 4.475 eV. Furthermore, 250 nm Al source/drain electrodes are employed. The device employs a DMG structure comprising Ag and Al as metals (M1 & M2), each of 500 nm, respectively. They are located on the drain–source sides, respectively. DMG provides a higher I_{ON}/I_{OFF} ratio [27], which is beneficial while building up long-term potentiation and depression performance. The 100 nm thick Al_2O_3 layer beneath the IGZO channel acts both as a gate dielectric and an ion-conducting electrolytic film. The Al_2O_3-based proton conducting electrolyte is modelled and simulated by the generic ion transport model. Thus, protons are present in the Al_2O_3 electrolyte of the DMG synaptic transistor, as shown in Fig. 2(a). As illustrated in Fig. 2(b), the dynamic EDL capacitive coupling is made possible by the diffusion of protons to the Al_2O_3/IGZO interface when a positive gate voltage is applied, increasing the number of electrons in the IGZO channel. To carry out the simulation analysis of the device, Silvaco ATLAS simulation software [31] has been used, incorporated with the FERMI and SRH models.

Fig. 3(a) shows the drain current versus gate voltage characteristics of the a-IGZO synaptic device calibrated with the experimental results [26], which shows the device design is in line with the experimental device. Fig. 3(b) shows the gate leakage characteristics of the device obtained by plotting J_{leak} versus voltage. The conductivity of the a-IGZO channel layer is treated as the synaptic weight to simulate neural stimulation and synaptic processes. Its variation leads to neural actions like short and long-term potentiation. The pulsating gate–drain voltage is regarded as the presynaptic input signal, while the drain–source current is the postsynaptic output signal of the device. These voltages have been chosen according to the type of plasticity needed to be observed in the device.

III. Results and Discussion

Synaptic behaviors in human memory are classified into STP and long-term plasticity (LTP). Long-term potentiation and depression are the two branches of LTP. The synaptic retention time segregates between STP and LTP. STP relates to the computational power of the human brain and can last over a few tens of milliseconds when a single input signal is fed to it. When the data are to be retained by a human brain over a more extended period, repeated stimuli or rehearsal form the foundation of the synaptic transition of STP to LTP. LTP is linked to the roots of memory and learning.

A. Short Term Plasticity

To study the STP performance, a single pulse (2 V, 1 ms) is used as the presynaptic input. It is applied to the DMG, which serves as the presynaptic input. The excitatory postsynaptic current (EPSC) (drain current), regarded as the postsynaptic output, shows a sudden rise in current when the pulse is applied. The above simulation is carried out at a drain voltage of 0.5 V. This rise in current is due to the increased conductivity of the IGZO channel layer as more protons move near the channel and electrolyte interface forming an EDL layer. Since this outcome is achieved by modulating channel conductivity, we refer to it as the synaptic weight. It is noticed that the EPSC reaches a maximum value of 0.96 μA and eventually decays over time to reach its initial value. Fig. 4(a) shows the simulated data of a single pulse simulation. The biological synapse shows similar behavior to STP, which lasts for a few milliseconds due to the increased neurotransmitters when the presynaptic neuron receives an input.

The energy consumption for the STP event can be calculated using by the following equation:

$$E = V_d \times I_{dm} \times T_{\text{Pulse}} \quad (1)$$

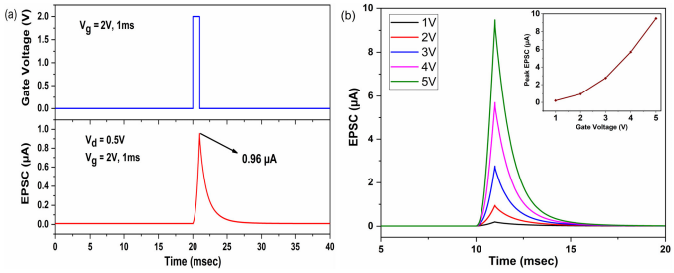

Fig. 4. (a) EPSC characteristics of the DMG device for a presynaptic gate pulse (2 V, 1 ms) at $V_d = 0.5$ V. (b) Drain current and presynaptic gate pulse relationship of different magnitudes ($V_g = 1$ to 5 V, 1 ms). (inset) Peak EPSC plotted against gate voltage amplitude.

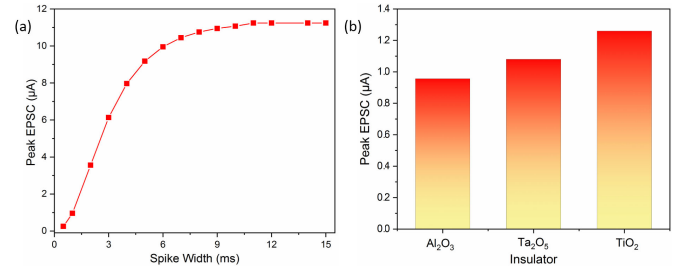

Fig. 5. (a) Relationship between peak EPSC and spike width for a single presynaptic gate voltage of 1 V at $V_d = 0.5$ V. (b) Peak EPSC variation with high-K dielectric as ion conducting electrolyte medium.

where V_d is the applied drain voltage, I_{dm} is the EPSC peak value, and T_{Pulse} is the time-period of the pulse. The device consumes 0.48 nJ of energy for the applied pulse. For a drain voltage of 0.1 V, the device consumes 0.03 pJ of energy.

Fig. 4(b) shows the application of gate voltage from 1 to 5 V at a constant drain voltage of 0.5 V, and their corresponding EPSC is plotted against time. As the gate voltage increases, peak EPSC rises from 0.198 to 9.47 μA. This rise in current is a linear function of the voltage, as shown in the inset of Fig. 4(b). The aforementioned behavior may be explained by the fact that as the gate pulse voltage is raised, protons from the ion-conducting electrolyte build up and create an EDL layer close to the interface, which further increases the channel's conductivity. Again, the ions lose energy and return to their initial positions when the pulse is withdrawn, which lowers the conductivity of the channel. Hence, the current settles down to its initial value. This behavior supports the idea that changes in amplitude can affect the STP synaptic response.

The variation of peak EPSC with spike width is illustrated in Fig. 5(a). There is a linear increase of peak EPSC for spike width varying between 0.5 to 8 ms, and it gets saturated at 11.27 μA for a spike width of 15 ms. The EPSC value increases with spike duration as more charges are created at the channel/electrolyte interface, which the trapping states capture. The charge-trapping states slowly get filled up with increasing pulsewidth. Since the charge remains constant, the current reaches a fixed value, and the peak EPSC saturates. Fig. 5(b) shows a comparative study on the peak value of EPSC if high-K dielectrics were used. It is noticed from Fig. 5(b) that a higher current would flow through the device, increasing its energy consumption [25]. This is due to the increased gate capacitance caused by the larger dielectric constant which leads to the rise of the inversion charge. Thus, a higher drain current occurs from an increase in inversion charge.

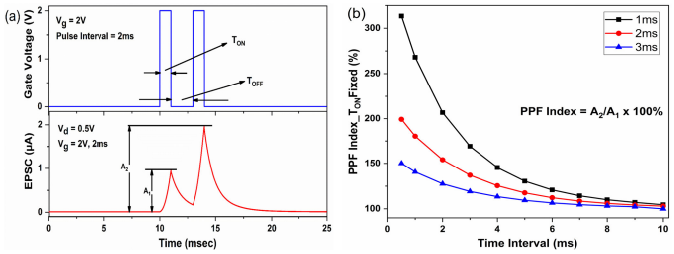

Fig. 6. (a) PPF for the DMG device triggered by two gate pulse (2 V, 2 ms). (b) PPF Index plotted against time interval keeping T_{ON} (pulsewidth) constant.

An important parameter in determining the strength of STP is paired-pulse facilitation (PPF), which also aids in deciphering auditory or visual cues [28]. As illustrated in Fig. 6(a), the PPF behavior of the device is examined by applying two equal pulsed gate voltages of magnitude 2 V and a pulse interval of 2 ms. It can be observed that the second pulse triggers a higher peak EPSC than the first peak. This higher EPSC value is the consequence of the second pulse firing, which happens much sooner than the ion relaxation. This makes it easier for the leftover ions from the initial pulse to be added to the ions that have already accumulated thereby increasing the amplitude of the drain current. The PPF Index is calculated as follows:

$$\text{PPF} = (A_2/A_1) \times 100\% \tag{2}$$

where, A_1 and A_2 are the first and second EPSC amplitude, respectively. The T_{OFF} (time interval) is varied, keeping the ON time fixed to obtain the PPF Index, as shown in Fig. 6(b). The graphs plotted are for three ON time intervals, viz. 1, 2, and 3 ms. PPF Index attains a maximum value of 310% for an ON time of 1 ms. The postsynaptic current produced by the first pulse does not fully return to the starting condition when the pulse is applied. As a result, when the subsequent pulse is used, it causes a rapid increase in postsynaptic current when the interval time is shorter. The first postsynaptic current is entirely restored when the interval duration is substantially longer. The following postsynaptic current will not differ considerably from the previous one as there are no excess residual protons at the channel/electrolyte interface. Therefore, as the time interval or pulsewidth increases, the PPF Index becomes stable at about 100%, indicating no change in peak EPSC of first and second pulse.

The PPF Index variation can be fitted into a double exponential curve [29] described as follows:

$$\text{PPF} = 1 + A_1 \exp\left(-t/\tau_1\right) + A_2 \exp\left(-t/\tau_2\right) \tag{3}$$

where A_1 and A_2 are the initial facilitation magnitudes of the rapid and slow phases, respectively; t is the amount of time between the two applied gate pulses; τ_1 and τ_2 are the relaxation times of the rapid and slow phases, respectively. From Fig. 6(b), for a time interval of 1 ms, the values of the curve fitting equations are calculated as follows: $A_1 = 151.43\%$, $A_2 = 120.94\%$, $\tau_1 = 1.596$ ms, $\tau_2 = 3.137$ ms. The measured values are comparable to biological synapses [30].

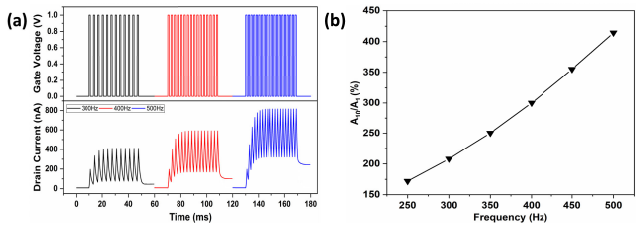

Fig. 7. (a) Potentiation formation by SRDP. Application of high-frequency presynaptic gate pulses (1 V, 1 ms) by varying frequency. (f = 300, 400, 500 Hz). (b) EPSC Gain (A_{10}/A_1) * 100% plotted as a function of frequency.

B. Potentiation Characteristics

The basis of long-term memory in the human brain is created by repeated events (stimuli) that cause lasting changes in synaptic connections. The two methods of studying the potentiation formation are spike-timing-dependent plasticity (STDP) and spike-rate-dependent plasticity (SRDP). STDP gives us an idea about the relationship between time intervals and drain current. In SRDP, the frequency of presynaptic spikes controls the variation in synaptic weight.

To study the formation of potentiation in our device, a high-frequency presynaptic pulse of 1 V is applied to the gate terminal of the device. Fig. 7(a) shows the STP to LTP transition when a train of pulses at frequencies of 300, 400, and 500 Hz is applied. It also shows the application of SRDP on our device. When a higher frequency stimulus is applied, the change in drain current is higher indicating the strengthening of potentiation. Since the pulses appear frequently with higher frequencies, there is not enough time for the conducting ions to lose energy and settle down. The application of the next pulse adds to the charge carriers in the device, which in turn increases the current. Hence, an increase in the frequency of the applied pulse results in strong LTP formation in our device which is a similar operation in the human brain. Fig. 7(b) shows the EPSC gain of the device. The EPSC can be modulated from 172% to 415% for a frequency change of 250 to 500 Hz. The EPSC gain curve supports that potentiation develops strength as frequency increases. The role of STDP in modulating the synaptic strength of the device is depicted in Fig. 8. A gate pulse (1 V, 250 Hz) is applied to simulate potentiation in the device. Varying the time interval as shown in Fig. 8(a)–(d), the LTP at time intervals of 1, 2, 3, and 3.5 ms is studied. The final peak drain current achieved after applying ten presynaptic pulses is of higher magnitude when the pulse interval is shorter. The drain current to which the characteristics settle after removal of the spike train also increases with increased frequency. Since the current does not decay to zero after removal of the pulse, it indicates the formation of potentiation in our device. Thus, STDP plays a vital role in forming LTP in the device.

Table I shows the effect of the change in pulse interval on the long-term potentiation of the device. A higher synaptic strength of 96% can be observed with the least off time which indicates the strength in LTP formation. This change in current also reflects the modulation of synaptic weight. % LTP Strength Index (4) calculates the strength of potentiation formation

$$\%\ \text{LTP Strength Index} = \frac{I_{d(\Delta t)} - I_{d(3.5\ \text{ms})}}{I_{d(\Delta t)}} \times 100\% \quad (4)$$

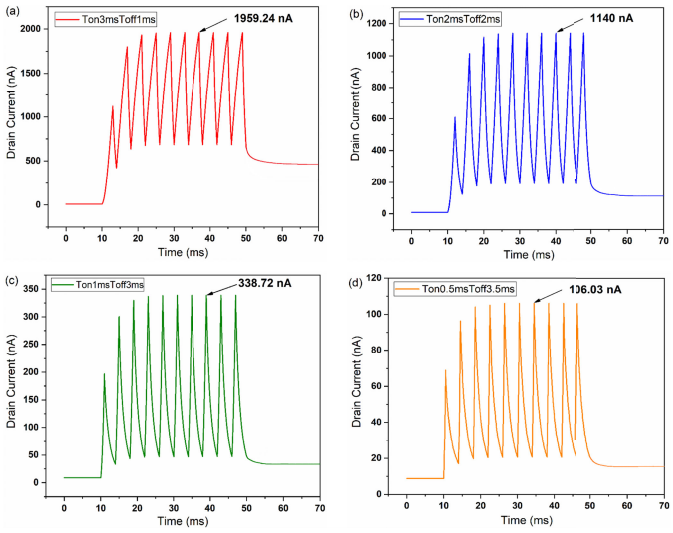

Fig. 8. Illustration of potentiation by STDP on application of a series of presynaptic pulses of 1 V magnitude and 250 Hz frequency. Drain current versus transient time. (a) Time interval of 1 ms. (b) Time interval of 2 ms. (c) Time interval of 3 ms. (d) Time interval of 3.5 ms.

TABLE I
FINAL DRAIN CURRENT, TIME INTERVAL, AND LTP STRENGTH INDEX ILLUSTRATING POTENTIATION PERFORMANCE AT 1 V, 250 Hz

Gate Voltage (V) & Frequency (Hz)	Time Interval (ms)	Final Drain Current (nA)	LTP Strength Index (%)
1 V, 250 Hz	1	436.78	95.99
	2	118.18	85.19
	3	28.7	39.02
	3.5	17.5	-

where, $I_{d(\Delta t)}$ is the final drain current at which it has settled after removal of pulse for Δt time interval, and $I_{d(3.5\ \text{ms})}$ is the final drain current at which it has settled after removal of pulse for 3.5 ms time interval. The dual metal used facilitates a higher ON/OFF current difference in the device, thus the regulation obtained in the device is so high that it facilitates a strong LTP formation.

C. Depression Characteristics

A presynaptic spike train is applied to the device's drain terminal while maintaining the gate and source terminals shorted. The postsynaptic output is regarded as the output of the short circuit terminals, which defines the depression characteristics of the device.

A presynaptic pulse of amplitude 1 V is applied at different frequencies of 250, 400, and 500 Hz at the drain terminal. Fig. 9 shows the gradual decrease in drain current with time for the simulated frequencies. This phenomenon occurs in the device due to the drifting of protons to the electrode and electrolyte interface. Due to the very high relaxation time, there is a gradual decrease in the drain current. It has been observed that with an increase in the frequency of the presynaptic input, the time taken by the drain current to reach its steady state increases.

Fig. 9 also shows the depression current reaching a steady state after the third, fifth, and sixth presynaptic pulses for frequencies of 250, 400, and 500 Hz.

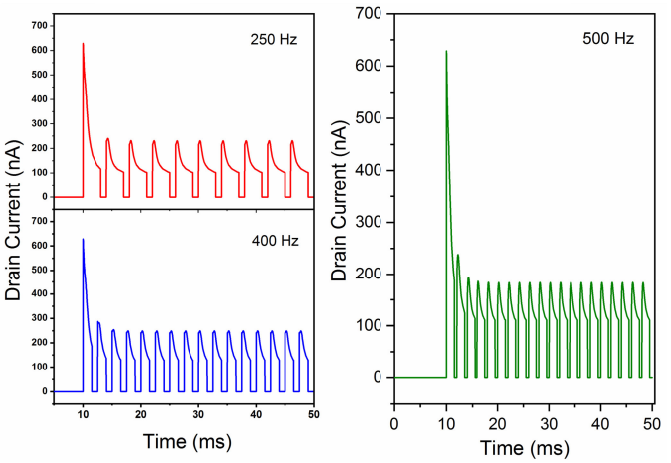

Fig. 9. Simulation of synaptic depression in DMG-based EDL device when a presynaptic drain spike train of 1 V (250, 400, and 500 Hz) is applied.

TABLE II
MAXIMUM AND MINIMUM DRAIN CURRENT, FREQUENCY, AND DUTY CYCLE ILLUSTRATING DEPRESSION PERFORMANCE

Frequency (Hz)	Duty Cycle	Max. Drain Current (nA)	Min. Drain Current (nA)	Depression Strength Index (%)
250	0.25	629.05	537.069	14.62
	0.5	629.05	397.6	36.79
	0.75	629.05	230.88	63.29
400	0.4	629.05	364.4	42.07
	0.6	629.05	248.01	60.57
	0.8	629.05	186.54	70.35
500	0.25	629.05	434.12	30.99
	0.5	629.05	257.61	59.05
	0.75	629.05	181.96	71.07

The synaptic strength during depression is calculated from the (%) current regulation as in the following equation:

$$\%\ \text{Depression Strength index} = \frac{I_{dmx} - I_{dmn}}{I_{dmx}} \times 100\% \quad (5)$$

where I_{dmx} is the peak current after first pulse and I_{dmn} is the peak value drain current when a steady state is reached. Table II shows an increase in synaptic strength with increased time interval, the depression characteristics of the device build up gradually. The DMG gate causes a decrease in $I_{d(\min)}$, which improves the drain current control and validates the degree of depression in our device. For a frequency of 500 Hz with a duty cycle of 0.75, the energy consumption calculated is estimated at 0.273 pJ from (1).

D. Filtering and Conductance Characteristics

Dynamic filtering characteristics, which represent the short-term behavioral study of the human brain in our device, are studied in this section. Filtering is an action of repeated learning caused by pulses of different frequencies. A spike train of presynaptic input of frequencies varying between 50 to 250 Hz is applied to study the EPSC behavior of the device, as shown in Fig. 10(a). The pulse train for each frequency consists of five consecutive pulses. It shows a gradual increase of the EPSC magnitude with increased frequency because the accumulated protons do not find enough time to drift back to their original state. However, the peak EPSC for a 50 Hz presynaptic input remains constant at around 200 nA for all five consecutive pulses because there is enough time for the protons to diffuse back to their initial state. This indicates that our device can act as a high-pass filter, which is of immense importance for transmitting and handling data in neuromorphic systems. The EPSC gain of the device is calculated as (A_{10}/A_1) and shows a rise from 100.2% to 171.82% for a frequency range of 50–250 Hz. The rise in gain with the rise in applied gate voltage is indicated by Fig. 10(b), confirms neurotransmitters' regulation between presynaptic input and postsynaptic response. It strengthens the process of dynamic filtering in our device. Fig. 10(c) is plotted to show the conductance characteristics of the device at a voltage of 1 V. Table III shows the performance parameters of our modelled device compared with IGZO-based experimental setups explored in recent publications. The device proposed in this work can reproduce all the synaptic behaviors compared to others. A substantial PPF percentage compared to its peers

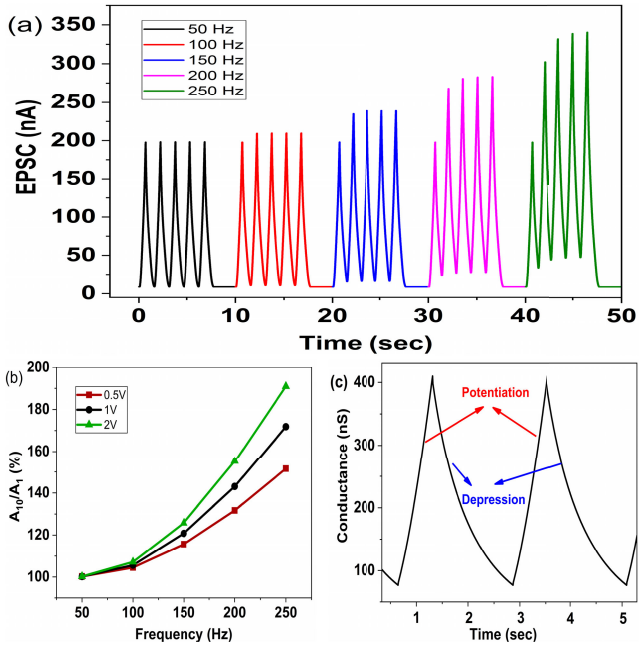

Fig. 10. (a) Mechanism of high pass filtering shown by the EPSC curve. (b) A_{10}/A_1 percentage as a function of increasing presynaptic voltage. (c) Conductance curve showing the potentiation and depression behaviors in the DMG EDL device.

TABLE III
BENCHMARK COMPARISON OF THE PERFORMANCE OF THE PROPOSED DEVICE

Reference	Dielectric Material	Compared Synaptic Parameters
[9]	SiO_2	PPF Index: 111% EPSC Gain: 101% to 139%
[18]	HfO_2	Depression Energy: 2.4 pJ
[32]	Nanogranular SiO_2	STP Energy Consumption = 1.08 pJ
[33]	Al_2O_3	STP Voltage < 9V LTP Voltage > 10V
This work	Nanogranular Al_2O_3	PPF Index: 315% EPSC Gain: 172% to 414% Depression Energy: 0.273 pJ V_d = 0.5 V, V_g =1 V STP Energy Consumption = 0.03 pJ

makes it suitable for enhanced potentiation and depression. The device also consumes low energy at all the stages of artificial synaptic memory.

IV. Conclusion

To simulate the behaviors of a human brain, a DMG IGZO device has been modelled and simulated in this work. Aluminum has been used widely in the simulation in the form of oxide and metals for the source, drain, and gate to reduce the cost of the device when manufactured. The short-term and long-term potentiation and depression characteristics are studied thoroughly, and their interdependence on frequency and pulsewidth are studied. PPF index attains a more than 300% value, far greater than IGZO-based EDL devices studied earlier. Filtering characteristics have shown the device to block all frequencies below and equal to 50 Hz. The dual metal strengthens the potentiation and depression formation in the device which has been calculated by the drain current regulation technique while maintaining a very low power consumption of 0.03 pJ. A tunable synaptic characteristic can be obtained by modulating the applied frequency and pulsewidth. The proposed model shows great potential for physical modelling and developing neuromorphic systems.

References

[1] J. Yang et al., "Neuromorphic engineering: From biological to spike-based hardware nervous systems," *Adv. Mater.*, vol. 32, no. 52, Dec. 2020, doi: 10.1002/adma.202003610.

[2] A. Sebastian, M. Le Gallo, R. Khaddam-Aljameh, and E. Eleftheriou, "Memory devices and applications for in-memory computing," *Nature Nanotechnol.*, vol. 15, no. 7, pp. 529–544, Jul. 2020, doi: 10.1038/s41565-020-0655-z.

[3] Y. Yang et al., "Long-term synaptic plasticity emulated in modified graphene oxide electrolyte gated IZO-based thin-film transistors," *ACS Appl. Mater. Interfaces*, vol. 8, no. 44, pp. 30281–30286, Nov. 2016, doi: 10.1021/acsami.6b08515.

[4] X. Wan, Y. Yang, Y. He, P. Feng, W. Li, and Q. Wan, "Neuromorphic simulation of proton conductors laterally coupled oxide-based transistors with multiple in-plane gates," *IEEE Electron Device Lett.*, vol. 38, no. 4, pp. 525–528, Apr. 2017, doi: 10.1109/LED.2017.2665578.

[5] H. Duan, L. Liang, Z. Wu, H. Zhang, L. Huang, and H. Cao, "IGZO/$CsPbBr_3$-nanoparticles/IGZO neuromorphic phototransistors and their optoelectronic coupling applications," *ACS Appl. Mater. Interfaces*, vol. 13, no. 25, pp. 30165–30173, Jun. 2021, doi: 10.1021/acsami.1c05396.

[6] H. Mao et al., "A spiking stochastic neuron based on stacked InGaZnO memristors," *Adv. Electron. Mater.*, vol. 8, no. 2, Feb. 2022, doi: 10.1002/aelm.202100918.

[7] W. Wang et al., "Investigation of light-stimulated a-IGZO based photoelectric transistors for neuromorphic applications," *IEEE Trans. Electron Devices*, vol. 67, no. 8, pp. 3141–3145, Aug. 2020, doi: 10.1109/TED.2020.3001492.

[8] S. Ke et al., "BCM learning rules emulated by a-IGZO-based photoelectronic neuromorphic transistors," *IEEE Trans. Electron Devices*, vol. 69, no. 8, pp. 4646–4650, Aug. 2022, doi: 10.1109/TED.2022.3178967.

[9] Y. M. Fu et al., "Sputtered oxide thin-film transistors with tunable synaptic spiking behavior at 1 V," *IEEE Trans. Electron Devices*, vol. 68, no. 6, pp. 2736–2741, Jun. 2021, doi: 10.1109/TED.2021.3075174.

[10] J. Sun, J. Jiang, A. Lu, and Q. Wan, "One-volt oxide thin-film transistors on paper substrates gated by SiO_2-based solid electrolyte with controllable operation modes," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2258–2263, Sep. 2010, doi: 10.1109/TED.2010.2052168.

[11] X. Wan, P. Feng, G. Dong Wu, Y. Shi, and Q. Wan, "Simulation of laterally coupled $InGaZnO_4$-based electric-double-layer transistors for synaptic electronics," *IEEE Electron Device Lett.*, vol. 36, no. 2, pp. 204–206, Feb. 2015, doi: 10.1109/LED.2015.2388952.

[12] H. Du, X. Lin, Z. Xu, and D. Chu, "Electric double-layer transistors: A review of recent progress," *J. Mater. Sci.*, vol. 50, no. 17, pp. 5641–5673, Sep. 2015, doi: 10.1007/s10853-015-9121-y.

[13] C. Wan, K. Xiao, A. Angelin, M. Antonietti, and X. Chen, "The rise of bioinspired ionotronics," *Adv. Intell. Syst.*, vol. 1, no. 7, Nov. 2019, Art. no. 1900073, doi: 10.1002/aisy.201900073.

[14] C. J. Wan, Y. H. Liu, L. Q. Zhu, P. Feng, Y. Shi, and Q. Wan, "Short-term synaptic plasticity regulation in solution-gated indium–gallium–zinc-oxide electric-double-layer transistors," *ACS Appl. Mater. Interfaces*, vol. 8, no. 15, pp. 9762–9768, Apr. 2016, doi: 10.1021/acsami.5b12726.

[15] T. Kamiya and H. Hosono, "Material characteristics and applications of transparent amorphous oxide semiconductors," *NPG Asia Mater.*, vol. 2, no. 1, pp. 15–22, Jan. 2010, doi: 10.1038/asiamat.2010.5.

[16] Y. Zeng et al., "Solution-processed InGaZnO-based artificial neuron for neuromorphic system," *IEEE Trans. Electron Devices*, vol. 70, no. 4, pp. 2170–2174, Apr. 2023, doi: 10.1109/TED.2023.3247363.

[17] J. Zhou, N. Liu, L. Zhu, Y. Shi, and Q. Wan, "Energy-efficient artificial synapses based on flexible IGZO electric-double-layer transistors," *IEEE Electron Device Lett.*, vol. 36, no. 2, pp. 198–200, Feb. 2015, doi: 10.1109/LED.2014.2381631.

[18] J. Wang, Y. Li, C. Yin, Y. Yang, and T.-L. Ren, "Long-term depression mimicked in an IGZO-based synaptic transistor," *IEEE Electron Device Lett.*, vol. 38, no. 2, pp. 191–194, Feb. 2017, doi: 10.1109/LED.2016.2639539.

[19] M. Madadi Asl, A.-H. Vahabie, A. Valizadeh, and P. A. Tass, "Spike-timing-dependent plasticity mediated by dopamine and its role in Parkinson's disease pathophysiology," *Frontiers Netw. Physiol.*, vol. 2, Mar. 2022, Art. no. 817524, doi: 10.3389/fnetp.2022.817524.

[20] P. L. Cardozo, I. B. Q. de Lima, E. M. A. Maciel, N. C. Silva, T. Dobransky, and F. M. Ribeiro, "Synaptic elimination in neurological disorders," *Current Neuropharmacol.*, vol. 17, no. 11, pp. 1071–1095, Oct. 2019, doi: 10.2174/1570159x17666190603170511.

[21] O. Kwon, S. Oh, H. Park, S.-H. Jeong, W. Park, and B. Cho, "In-depth analysis on electrical parameters of floating gate IGZO synaptic transistor affecting pattern recognition accuracy," *Nanotechnology*, vol. 33, no. 21, May 2022, Art. no. 215201, doi: 10.1088/1361-6528/ac5444.

[22] Y. He et al., "IGZO-based floating-gate synaptic transistors for neuromorphic computing," *J. Phys. D, Appl. Phys.*, vol. 53, no. 21, May 2020, Art. no. 215106, doi: 10.1088/1361-6463/ab7bb4.

[23] L. Zhu, Y. He, C. Chen, Y. Zhu, Y. Shi, and Q. Wan, "Synergistic modulation of synaptic plasticity in IGZO-based photoelectric neuromorphic TFTs," *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp. 1659–1663, Apr. 2021, doi: 10.1109/TED.2021.3060687.

[24] R. R. Thakur and P. Singh, "Performance reliability of ultra-thin Si-SiO_2, Si-Al_2O_3, Si-ZrO_2 and Si-HfO_2 interface in rectangular steep retrograded nano-regimes devices," *Microelectron. Rel.*, vol. 96, pp. 21–28, May 2019, doi: 10.1016/j.microrel.2019.02.003.

[25] M. Aditya, K. S. Rao, K. G. Sravani, and K. Guha, "Simulation and drain current performance analysis of high-k gate dielectric FinFET," *Silicon*, vol. 14, no. 8, pp. 4075–4078, Jun. 2022, doi: 10.1007/s12633-021-01176-3.

[26] T.-C. Fung et al., "Two-dimensional numerical simulation of radio frequency sputter amorphous In–Ga–Zn–O thin-film transistors," *J. Appl. Phys.*, vol. 106, no. 8, Oct. 2009, Art. no. 084511, doi: 10.1063/1.3234400.

[27] S. Kale and M. S. Chandu, "Dual metal gate dielectric engineered dopant segregated Schottky barrier MOSFET with reduction in ambipolar current," *Silicon*, vol. 14, no. 3, pp. 935–941, Feb. 2022, doi: 10.1007/s12633-020-00921-4.

[28] R. S. Zucker and W. G. Regehr, "Short-term synaptic plasticity," *Annu. Rev. Physiol.*, vol. 64, pp. 355–405, Mar. 2002.

[29] F. Yu et al., "Chitosan-based polysaccharide-gated flexible indium tin oxide synaptic transistor with learning abilities," *ACS Appl. Mater. Interfaces*, vol. 10, no. 19, pp. 16881–16886, May 2018, doi: 10.1021/acsami.8b03274.

[30] L. Q. Zhu, C. J. Wan, L. Q. Guo, Y. Shi, and Q. Wan, "Artificial synapse network on inorganic proton conductor for neuromorphic systems," *Nature Commun.*, vol. 5, no. 1, Jan. 2014, doi: 10.1038/ncomms4158.

[31] *SILVACO: ATLAS Device Simulation Software*, Silvaco Int., Santa Clara, CA, USA, 2019.

[32] W. Cheng et al., "Proton conductor gated synaptic transistor based on transparent IGZO for realizing electrical and UV light stimulus," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 38–45, 2019, doi: 10.1109/JEDS.2018.2875976.

[33] D. Kang et al., "Short- and long-term memory based on a floating-gate IGZO synaptic transistor," *IEEE Access*, vol. 11, pp. 20196–20201, 2023, doi: 10.1109/ACCESS.2023.3249479.