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लिए अनुप्रयोग — दिशानिर्देश

### Insulation Co-Ordination Part 12 Application for LCC HVDC Converter Stations — Guidelines

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भारतीय मानक ब्यूरो

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## NATIONAL FOREWORD

This Indian Standard which is identical to IEC 60071-12 : 2022 'Insulation co-ordination — Part 12: Application guidelines for LCC HVDC converter stations' Issued by the International Electrotechnical Commission (IEC) was adopted by the Bureau of Indian Standards on the recommendation of the HVDC Power Systems Sectional Committee and approval of the Electrotechnical Division Council.

This standard supersedes IS/IEC 60071-5 : 2014 Insulation co-ordination: Part 5 Procedures for high-voltage direct current ( HVDC ) converter stations. 

This standard is published in various parts. Other parts in this series are:

- Part 1 Definition principles and rules
- Part 2 Application guide
- Part 4 Computational guide to insulation co-ordination and modeling of electrical networks
- Part 5 Procedures for high-voltage direct current (HVDC) converter stations

The text of the IEC standard has been approved as suitable for publication as an Indian Standard without deviations. Certain conventions are, however, not identical to those used in Indian Standards. Attention is particularly drawn to the following:

- a) Wherever the words 'International Standard' appears referring to this standard, they should be read as 'Indian Standard'; and
- b) Comma (,) has been used as a decimal marker, while in Indian Standards the current practice is to use a point (.) as the decimal marker.

In this adopted standard, reference appears to International Standards for which Indian Standards also exists. The corresponding Indian Standards, which are to be substituted, are listed below along with their degree of equivalence for the editions indicated:

<i>International Standard</i>	<i>Corresponding Indian Standard</i>	<i>Degree of Equivalence</i>
IEC 60099-4, Surge arresters — Part 4: Metal-oxide surge arresters without gaps for a.c. systems	IS 15086 (Part 4) : 2017/IEC 60099-4 : 2014 Surge arresters: Part 4 Metal-oxide surge arresters without gaps for a.c. systems	Identical
IEC 60633, High-voltage direct current (HVDC) transmission — Vocabulary	IS 14801 : 2021/IEC 60633 : 2019 High-voltage direct current HVDC transmission Vocabulary ( <i>first revision</i> )	Identical

The Committee has reviewed the provision of the following International Standard referred in this adopted standard and has decided that it is acceptable for use in conjunction with this standard:

<i>International Standard</i>	<i>Title</i>
IEC 60071-11	Insulation co-ordination – Part 11 : Definitions, principles and rules for HVDC system

Only English language text has been retained while adopting it in this Indian Standard, and as such the page numbers given here are not the same as in the International Standard.

For the purpose of deciding whether a particular requirement of this standard is complied with, the final value, observed or calculated expressing the result of a test, shall be rounded off in accordance with IS 2 : 2022 'Rules for rounding off numerical values (*second revision*)'. The number of significant places retained in the rounded off value should be the same as that of the specified value in this standard.

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*Indian Standard***INSULATION CO-ORDINATION****PART 12 APPLICATION FOR LCC HVDC CONVERTER STATIONS —  
GUIDELINES****1 Scope**

This part of IEC 60071 applies guidelines on the procedures for insulation co-ordination of line commutated converter (LCC) stations for high-voltage direct current (HVDC) project, whose aim is evaluating the overvoltage stresses on the converter station equipment subjected to combined DC, AC power frequency, harmonic and impulse voltages, and determining the specified withstand voltages for equipment.

This document deals only with metal-oxide surge arresters, without gaps, which are used in modern HVDC converter stations. The criteria for determining the protective levels of series and/or parallel combinations of surge arresters used to ensure optimal protection are also presented. Typical arrester protection schemes and stresses of arresters are presented.

Annex A contains examples of insulation co-ordination for LCC HVDC converters which support the concepts described in the main text, and the basic analytical techniques used.

**2 Normative references**

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60071-11<sup>2</sup>, *Insulation co-ordination – Part 11 : Definitions, principles and rules for HVDC system*

IEC 60099-4, *Surge arresters – Part 4: Metal-oxide surge arresters without gaps for a.c. systems*

IEC 60633, *High-voltage direct current (HVDC) transmission – Vocabulary*

**3 Terms, definitions, symbols and abbreviated terms****3.1 Terms and definition**

For the purposes of this document, the terms and definitions given in IEC 60071-11 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

<sup>2</sup> Under preparation. Stage at the time of publication: IEC/CFDIS 60071-11:2022.

### 3.1.1

#### **crest value of continuous operating voltage**

CCOV

highest continuously occurring crest value of the voltage at the equipment on the DC side of the converter station excluding commutation overshoots

### 3.1.2

#### **peak value of continuous operating voltage**

PCOV

highest continuously occurring crest value of the voltage at the equipment on the DC side of the converter station including commutation overshoots and commutation notches

### 3.1.3

#### **valve protective firing**

means of protecting the thyristors from excessive forward voltage, rate of change of voltage or forward voltage applied during the reverse recovery time, by firing the thyristors into conduction

## 3.2 Symbols and abbreviated terms

### 3.2.1 General

The list covers only the most frequently used symbols and abbreviated terms, some of which are illustrated graphically in the single-line diagram of Figure 1 and Figure 2. For a more complete list of symbols which has been adopted for LCC HVDC converter stations, and also for insulation co-ordination, refer to the standards listed in the normative references (Clause 2) and to the Bibliography.

### 3.2.2 Subscripts

0(zero)	at no load (IEC 60633)
d	direct current or voltage (IEC 60633)
i	ideal (IEC 60633)
max	maximum (IEC 60633)
n	pertaining to harmonic component of order n (IEC 60633)

### 3.2.3 Letter symbols

$K_a$	altitude correction factor (IEC 60071-1)
$K_c$	co-ordination factor (IEC 60071-1)
$K_s$	safety factor (IEC 60071-1)
$U_c$	continuous operating voltage of an arrester
$U_{ccov}$	crest value of continuous operating voltage
$U_{ch}$	continuous operating voltage of an arrester including harmonics
$U_{di0}$	ideal no-load direct voltage (IEC 60633)
$U_{di0max}$	maximum value of $U_{di0}$ taking into account AC voltage measuring tolerances, and transformer tap-changer offset by one step
$U_s$	highest voltage of an AC system (IEC 60071-1 and IEC 60071-2)
$U_m$	highest voltage for the equipment
$U_{v0}$	no-load phase-to-phase voltage on the valve side of converter transformer, r.m.s. value excluding harmonics



$U_{rp}$	representative overvoltage
$U_{cw}$	co-ordination withstand voltage
$U_{rw}$	required withstand voltage
$U_w$	specified withstand voltage (standard withstand voltage in alternating current)
$\alpha$	delay angle (IEC 60633); “firing angle” also used in this standard
$\beta$	advance angle (IEC 60633)
$\gamma$	extinction angle (IEC 60633)
$\mu$	overlap angle (IEC 60633)

### 3.2.4 Abbreviated terms

LCC	line commutated converter
VSC	voltage sourced converter
HVDC	high voltage direct current
HV	high voltage
LV	low voltage
CCOV	crest value of continuous operating voltage
GIS	gas-insulated switchgear
PCOV	peak continuous operating voltage
ECOV	equivalent continuous operating voltage
RSFO	representative slow-front overvoltage (the maximum voltage stress value)
RFFO	representative fast-front overvoltage (the maximum voltage stress value)
RSTO	representative steep-front overvoltage (the maximum voltage stress value)
RSIWV	required switching impulse withstand voltage
RLIWV	required lightning impulse withstand voltage
RSTIWV	required steep-front impulse withstand voltage
SIPL	switching impulse protective level
LIPL	lightning impulse protective level
STIPL	steep-front impulse protective level
SIWV	switching impulse withstand voltage
LIWV	lightning impulse withstand voltage
STIWV	steep-front impulse withstand voltage
p.u.	per unit

## 4 Typical LCC HVDC converter station schemes

Figure 1 shows the single line diagram of typical LCC HVDC converter stations equipped with two 12-pulse converters in series. It can be noted that Figure 1 shows possible arrester locations covered in this document. Some of these arresters can be redundant and could be excluded depending on the specific design.

Figure 2 shows an example for a single line diagram and arrester arrangement of a back-to-back converter station. Other arrangements with different earthing connections are also common, e.g., earthing at the mid-point between the two six-pulse bridges. The location of the smoothing reactor, if applicable, can change accordingly.

The AC and DC filter configurations could be more complex than those shown in these figures.

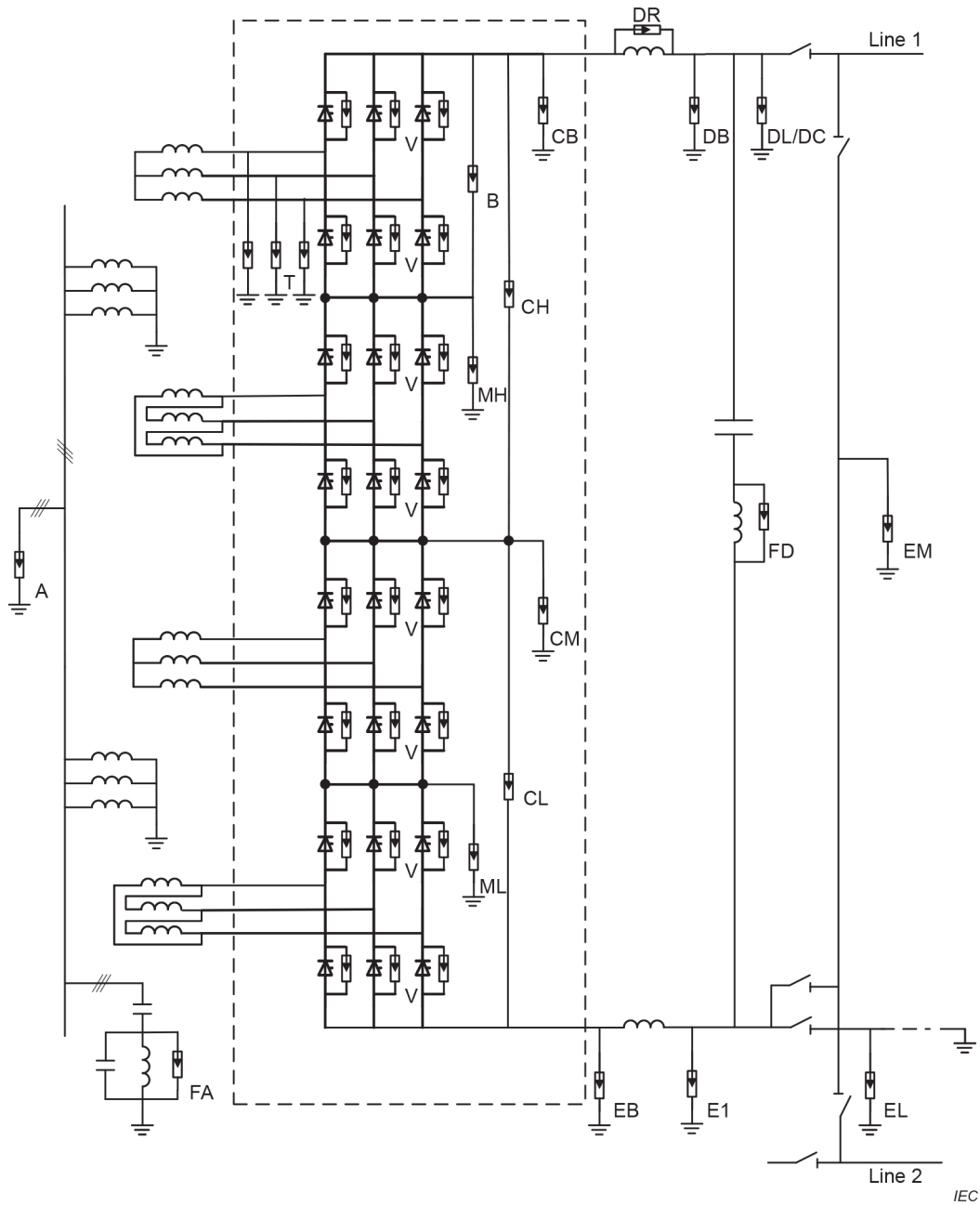
Table 1 presents the graphical symbols used in this document.

The thyristor valves being voltage sensitive require strict overvoltage protection, which is provided by valve arresters that are connected directly across the valve terminals.

The valve arresters in combination with other arresters typically provide protection to transformer valve windings and in general separate phase-phase and phase-earth arresters are not provided. Transformer valve winding phase-to-earth arresters can be considered at 800 kV and above to lower the insulation levels especially to the top valve group.

Each voltage level and component are protected by either a single arrester or a combination of series or parallel connected arresters.

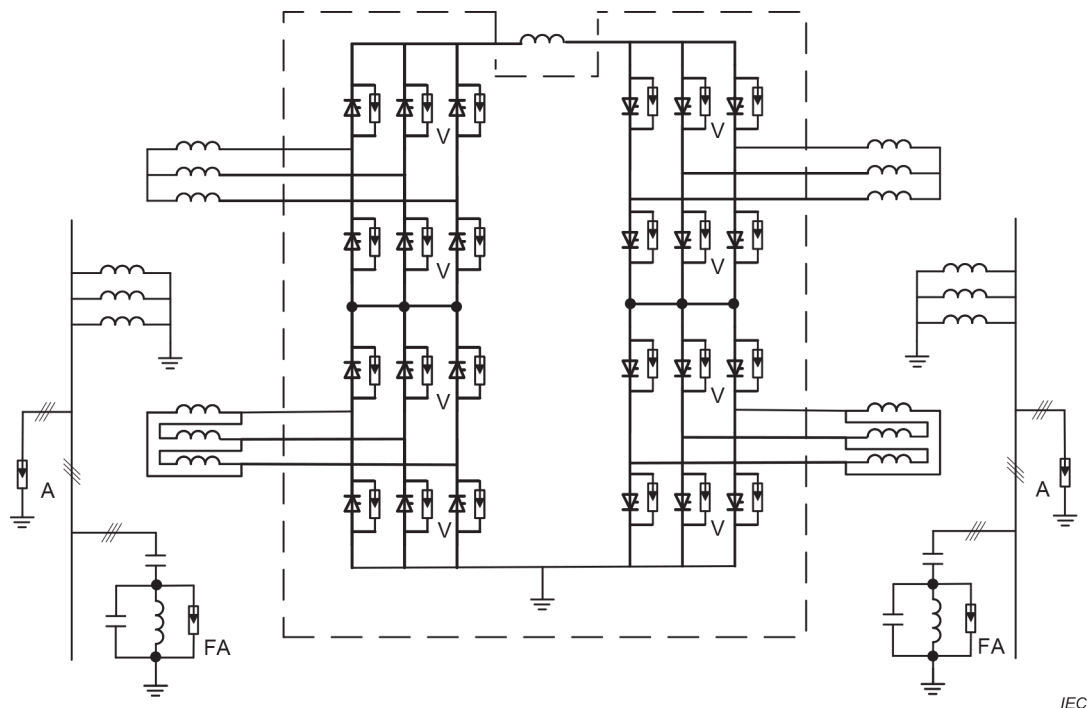
Arrester designations and details on their design and specific roles are presented in Clause 6.



**Key**

- |     |                                    |     |                                       |
|-----|------------------------------------|-----|---------------------------------------|
| A:  | AC bus arrester                    | FA: | AC filter arrester                    |
| FD: | DC filter arrester                 | EL: | electrode line arrester               |
| E1: | DC neutral bus arrester            | EM: | metallic return arrester              |
| EB: | converter neutral arrester         | B:  | bridge arrester (6-pulse)             |
| V:  | valve arrester                     | CB: | converter unit DC bus arrester        |
| T:  | transformer valve winding arrester | DB: | DC bus arrester                       |
| DR: | smoothing reactor arrester         | DC: | DC cable arrester                     |
| DL: | DC line arrester                   | CM: | arrester between converters unit      |
| CL: | LV converter unit arrester         | MH: | mid-point bridge arrester (HV bridge) |
| CH: | HV converter unit arrester         | ML: | mid-point bridge arrester (LV bridge) |

**Figure 1 – Possible arrester locations in a pole with two 12-pulse converters in series**



**Key**

A: AC bus arrester

FA: AC filter arrester

V: valve arrester

**Figure 2 – Possible arrester locations for a back-to-back converter station**

**Table 1 – Symbol description**

Symbol	Description
	Single valve (thyristor) IEC 60617-S00057:2001-07
	Arrester IEC 60617-S00373:2001-07
	Reactor IEC 60617-S00849:2001-07
	Capacitor IEC 60617-S00567:2001-07
	Earth IEC 60617-S00200:2001-07

**5 Voltages and overvoltages in service**

**5.1 Continuous operating voltages at various locations in the converter station**

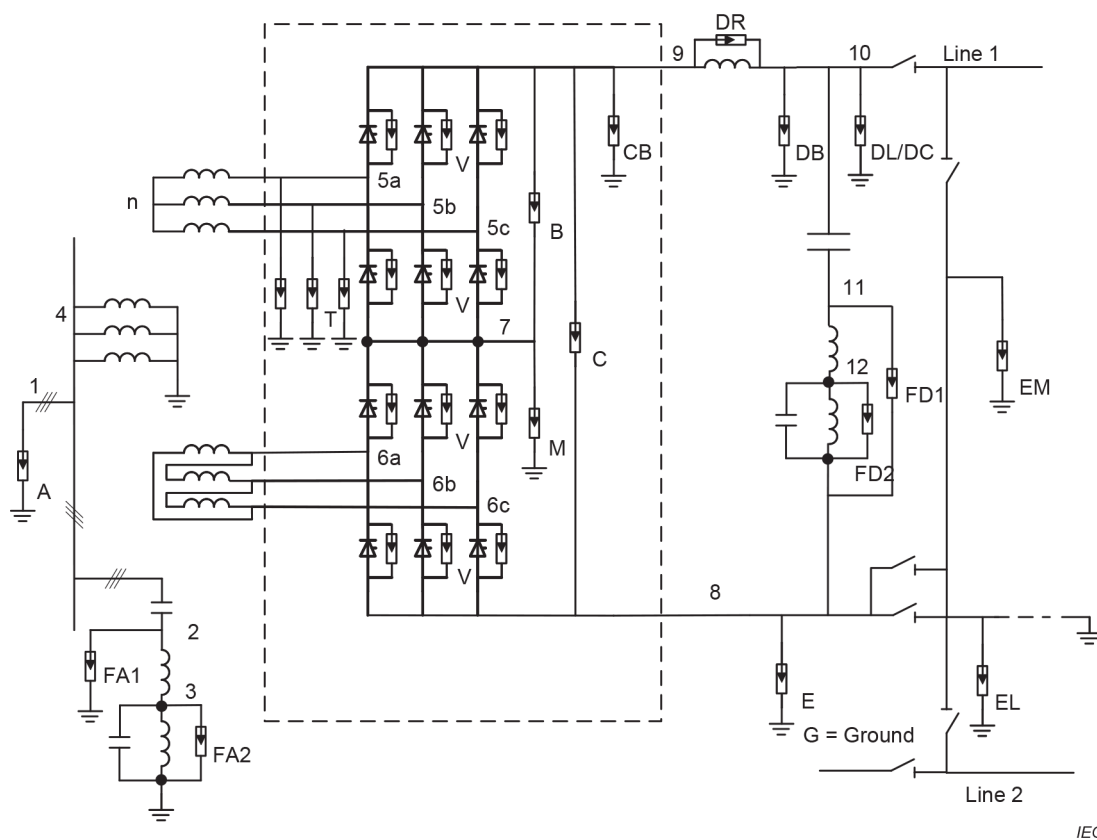
The continuous operating voltages at various locations in an LCC HVDC converter station differ from the AC system in that they consist of not simply the fundamental frequency voltages. They could be a combination of direct voltage, fundamental frequency voltage, harmonic voltages, and high frequency transients, depending upon the location.

Table 3 shows an LCC HVDC converter station in a pole with one 12-pulse converter configuration. In general phase-earth arresters on the valve side of the converter transformer (T) are not provided for LCC HVDC schemes up to 600 kV.

Figure 1 shows an LCC HVDC scheme with two 12-pulse converters in series per pole configuration, which has been used for the early 600 kV scheme and some 800 kV schemes.

Figure 4 shows typical waveforms of continuous operating voltages excluding commutation overshoots at various locations in the LCC HVDC converter station either to earth (G) or to another point for the typical configuration of Figure 3. The numbers and alphabetical designations, in Figure 3, identify node numbers and arrester designations respectively. These waveforms have been produced with a simulation tool considering typical DC parameters.

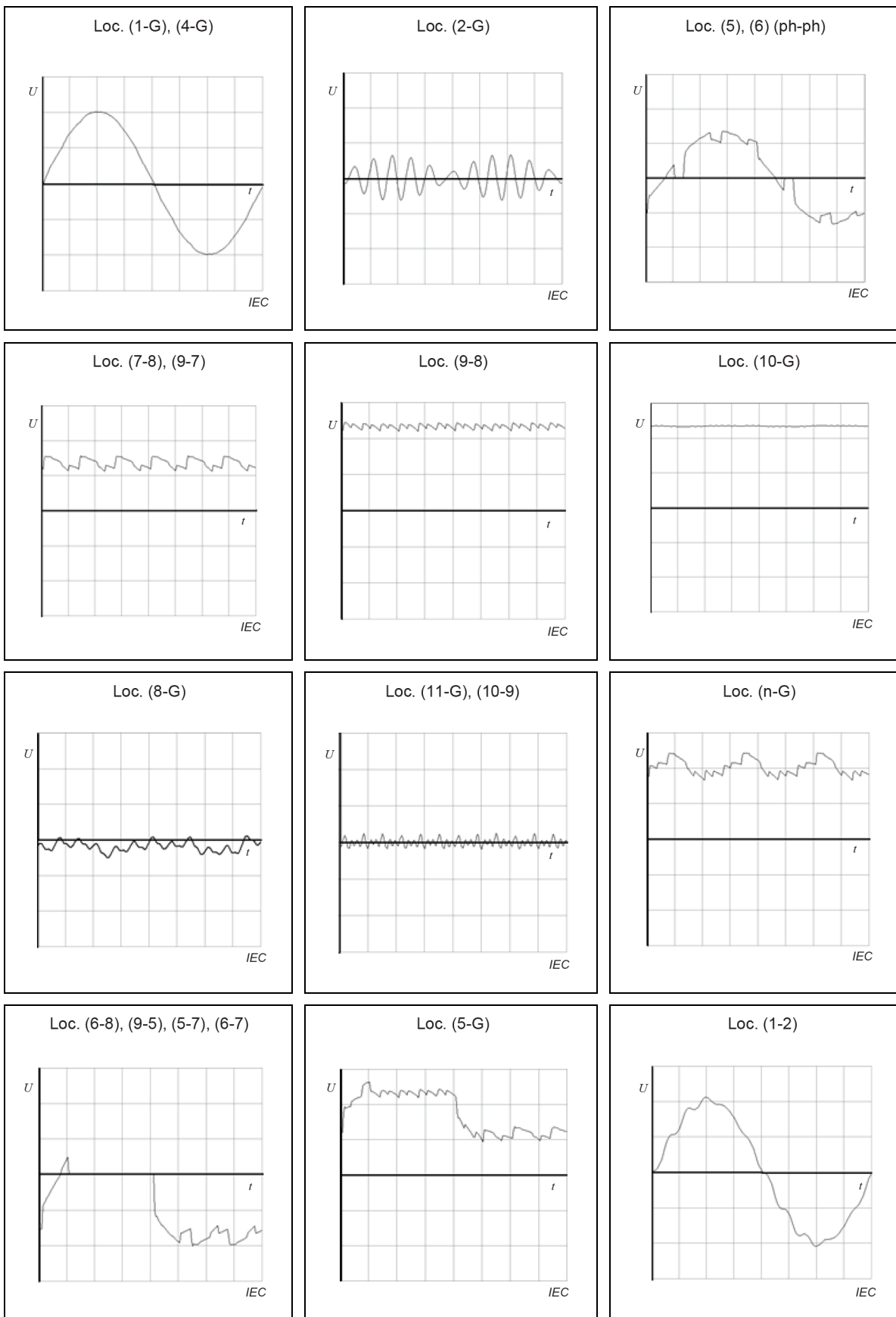
Note that Figure 1, Figure 2 and Figure 3 show possible arrester locations, and some of them can be eliminated because of specific designs.

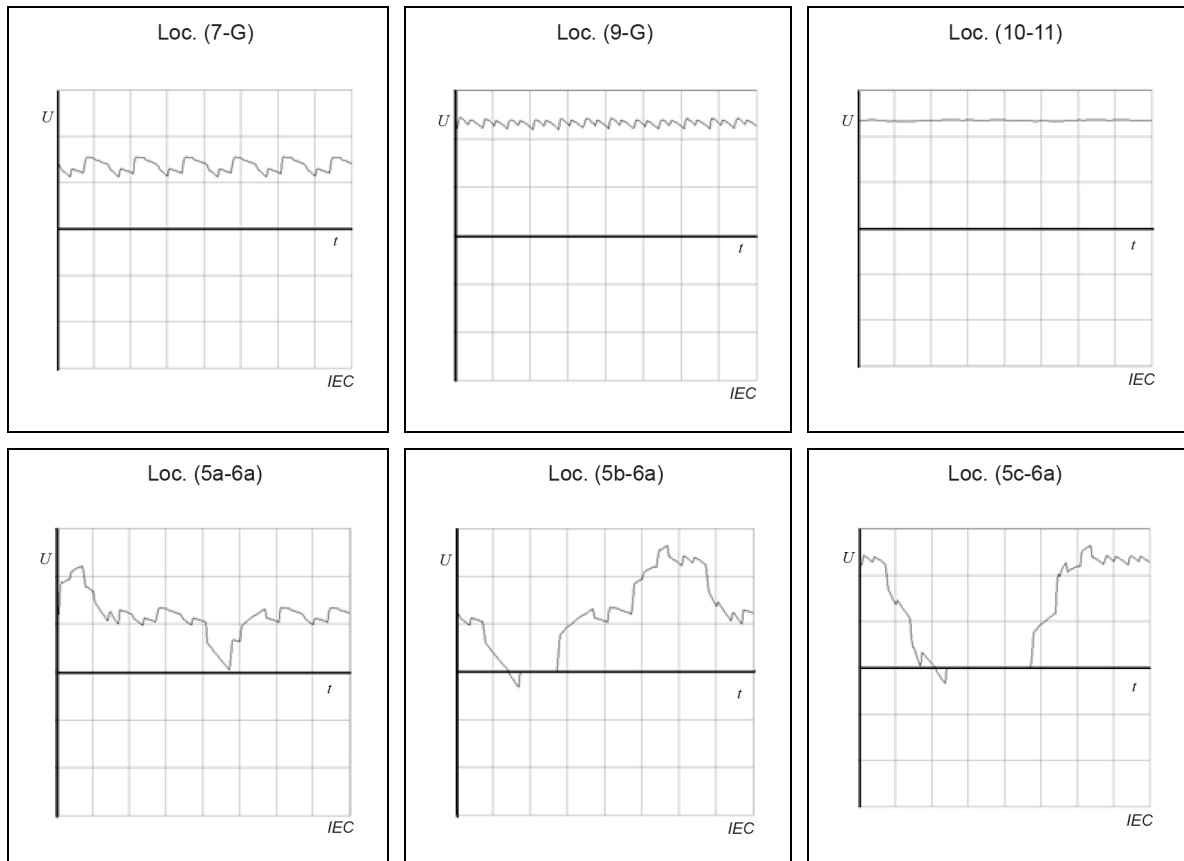


**Key**

- |           |                                    |           |                                |
|-----------|------------------------------------|-----------|--------------------------------|
| A:        | AC bus arrester                    | CB:       | converter unit DC bus arrester |
| M:        | mid-point bridge arrester          | EM:       | metallic return arrester       |
| E:        | DC neutral bus arrester            | EL:       | electrode line arrester        |
| V:        | valve arrester                     | B:        | bridge arrester (6-pulse)      |
| T:        | transformer valve winding arrester | C:        | converter unit arrester        |
| DR:       | smoothing reactor arrester         | DB:       | DC bus arrester                |
| DL:       | DC line arrester                   | DC:       | DC cable arrester              |
| FA1, FA2: | AC filter arresters                | FD1, FD2: | DC filter arresters            |

**Figure 3 – LCC HVDC converter station in a pole with one 12-pulse converter**





**Figure 4 – Continuous operating voltages at various locations  
(location identification according to Figure 3)**

The harmonics generated on the AC side are assumed to be filtered by the connected filters and thus the voltage at Loc. (1-G) and (4-G) is considered sine wave of fundamental frequency without any harmonics.

Voltage shape at Loc. (1-2) is also predominantly a fundamental frequency sine wave but superimposed by harmonics. The content of harmonics strongly depends on the filter configuration, tuning frequencies as well as operating condition of the converters. Typically, the content is less than 30 % of the fundamental frequency.

The voltages across the 6-pulse bridges (Loc. (7-8) and (9-7)) are the DC voltages across the bridges consisting of about  $60^\circ$  arcs of line-line AC voltages ( $60^\circ - \mu$ , duration) and the average of line-line voltages (duration,  $\mu$ ).

The voltage at the 6-pulse bridge to earth (Loc. (7-G)) can be identical to Loc. (7-8) if the station is earthed via the station earth as well as during symmetrical operation of a bipole. However, in case of unsymmetrical bipolar operation or monopolar operation an additional DC offset will be superimposed.

The voltage across the 12-pulse converter (Loc. (9-8)) comprises of  $30^\circ$  arcs of line-line AC voltages with superimposed influence of firing delay and overlap angles.

The voltage across the 12-pulse converter to earth (Loc. (9-G)) can be identical to Loc. (9-8) or include an additional dc offset due to the same reasons as described for Loc. (7-G) (see above).

Voltage shapes of Loc. (5b-6a) and (5c-6a) show the voltage between two different phases of the two six-pulse groups. This wave shape is relevant only in case of three-phase 3-winding transformers.

The voltage at Loc. (10-G) is the smoothed out voltage due to the influence of the smoothing reactor and DC filter, if applicable.

The voltages at Loc. (6-8) and (9-5) are the voltages across a valve in rectifier mode indicating the valve conduction period and commutation in its own row and the other row of thyristors in a 6-pulse bridge.

The voltage across the transformer valve winding phase-phase is shown in Loc. (5), (6) (ph-ph). The zero voltage shows the commutation process involving the valves connected to the corresponding two phases, while the notches indicate the commutation involving valves that are connected to one of the phases.

Neutral bus voltage (Loc. (8-G)) and voltages across the filters are indicative of typical voltages and they depend on electrode circuit and filter parameters. Loc. (8-G) can also include a DC offset especially during monopolar metallic return operation.

The voltage at location (n-G) has a DC component equal to 3/4 of pole voltage (Loc. (10-G)) plus the ripple of the lower 6-pulse bridge and half of the ripple of the upper 6-pulse bridge.

## 5.2 Peak continuous operating voltage (PCOV) and crest continuous operating voltage (CCOV)

The switching action of the valves produces high frequency turn-on and turn-off commutation transient voltages which are superimposed on the commutation voltage. The overshoot at turn off increases the transformer valve-side winding voltage and in particular the off-state (reverse-blocking) voltage across the valves and associated valve arresters. The amplitude of the overshoot is determined by:

- a) the inherent characteristics of the thyristors (particularly the recovery charge);
- b) the distribution of the recovery charge in a series-connected string of thyristors in a valve;
- c) the damping resistors and capacitors at individual thyristor levels;
- d) the various capacitances and inductances within the valve and commutation circuit;
- e) the firing and overlap angles;
- f) the valve commutation voltage at the instant of turn-off.

The continuous operating voltage waveform across the (Loc. (6-8) and (9-5)) and valve arrester (V), during rectifier operation, is shown in Figure 5.

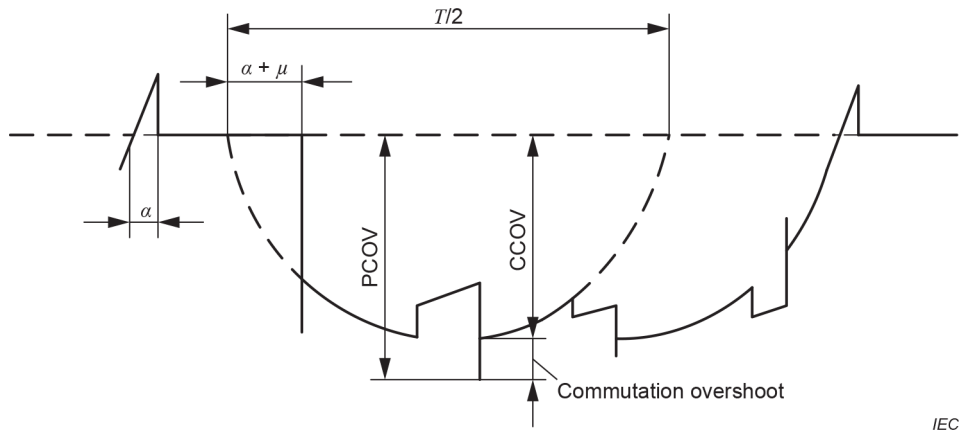
The CCOV (defined in Clause 3) is proportional to the  $U_{di0max}$ , and is given by:

$$U_{ccov} = \frac{\pi}{3} \cdot U_{di0max} = \sqrt{2} \cdot U_{v0}$$

Refer to 3.2.3 for the definition of  $U_{di0max}$  and  $U_{v0}$ .

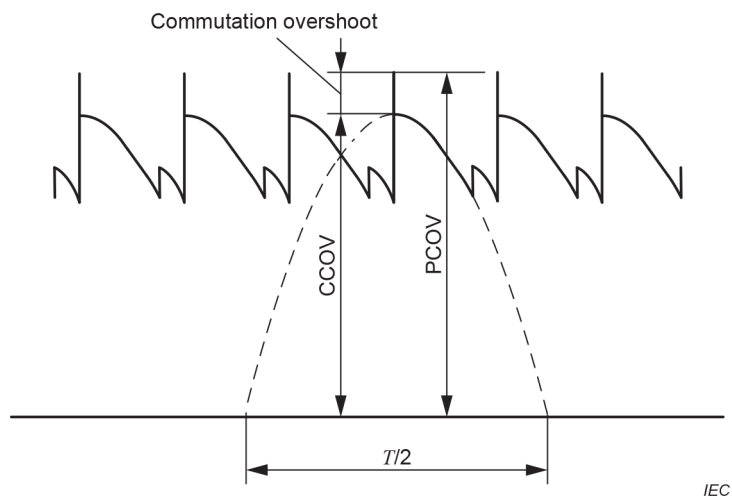
Operation with large delay angles  $\alpha$  increases the commutation overshoots, and special care shall be taken that these do not overstress the arresters.



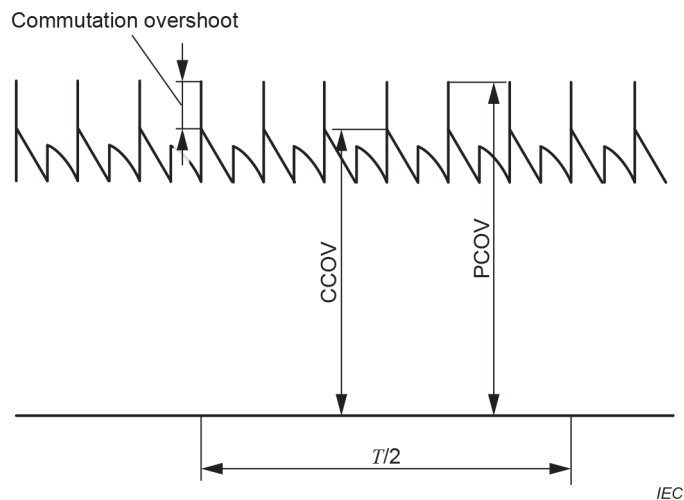


**Figure 5 – Operating voltage of a valve arrester (V), rectifier operation and definition of PCOV and CCOV**

The continuous operating voltage waveforms across the mid-point arrester (M) (Loc. (7-G)) and across the converter bus arrester (CB) (Loc. (9-G)) are shown in Figure 6 and Figure 7, respectively.



**Figure 6 – Operating voltage of a mid-point arrester (M), rectifier operation**



**Figure 7 – Operating voltage of a converter bus arrester (CB), rectifier operation**

### 5.3 Sources and types of overvoltages

Overvoltages on the AC side can originate from switching, faults, load rejection or lightning. The dynamic characteristics of the AC network, its impedance and also its effective damping at dominant transient oscillation frequencies, and the proper modelling of the converter transformers, static and synchronous compensators and the filter components, are important in evaluating the overvoltages. If the lengths of busbars in the AC switchyard are significant, they shall be taken into account in the evaluation of lightning and fast-front overvoltages (e.g., distance effects) and in the location of arresters.

Overvoltages on the DC side can originate from either the AC system or the DC line and/or cable, or from in-station flashovers. or other fault events.

In assessing the overvoltages, the configuration of the AC and DC systems shall be taken into account as well as the dynamic performance of the valves and controls, and credible worst case combinations, as discussed in Clauses 6 and 8.

Impacts on arrester requirements are discussed in Clause 6.

While the origin of overvoltages can result from different phenomena (switching, fault and lightning) and described above, the overvoltages are categorized according to their shape and duration as:

- temporary overvoltages (power frequency overvoltage of relatively long duration),
- transient overvoltages (short-duration overvoltage of few milliseconds or less, oscillatory or non-oscillatory, usually highly damped).

Transient overvoltages can be further classified as:

- slow front overvoltages,
- fast-front overvoltages,
- very-fast-front overvoltages,
- steep-front overvoltages.

### 5.4 Temporary overvoltage

#### 5.4.1 General

A temporary overvoltage is defined as an oscillatory overvoltage of relatively long duration which is undamped or only weakly damped. The temporary overvoltages can originate either from the AC side or the DC side.

#### 5.4.2 Temporary overvoltage on the AC side

These overvoltages are usually generated due to switching operations or faults. The highest temporary overvoltages usually occur in conjunction with sudden loss of load caused by faults either on the AC system or the DC system with AC reactive sources still connected. If the connected reactive elements and the AC system result in resonance conditions the temporary overvoltages can be more severe both from the overvoltage magnitude and arrester energy duty point of view.

Together with the highest AC operating voltages ( $U_s$ ), the temporary overvoltage will be decisive for setting the rated voltage of AC bus arresters (A).

Temporary overvoltages together with high firing or extinction angles should also be considered for valve arresters (V).

Temporary overvoltages due to AC side faults resulting in asymmetrical and distorted AC voltages result in second harmonic voltages on the DC side which in turn cause third harmonic voltages on the AC side stressing the AC filter arrester (FA). When the converters are blocked with firing pulses given to by-pass pairs, the arresters across the non-conducting valves can be exposed to phase-phase voltages.

#### **5.4.3 Temporary overvoltages on the DC side**

An uncontrolled energization of the rectifier with the far end being blocked could result in high overvoltages, especially for a cable transmission system.

Another case that can result in overvoltages is the blocking of an inverter at high current without firing of a by-pass pair. This will result in an application of fundamental frequency voltage at the inverter, and if the DC circuit is resonant close to the fundamental frequency, could result in high overvoltages stressing the DC bus arrester (CB).

### **5.5 Slow-front overvoltages**

#### **5.5.1 General**

Slow-front and temporary overvoltages occurring on the AC side are important to the study of arrester applications. Together with the highest AC operating voltages ( $U_s$ ) they determine the overvoltage protection and insulation levels of the AC side of the LCC HVDC converter station. They also influence valve insulation co-ordination.

#### **5.5.2 Slow-front overvoltages on the AC side**

##### **5.5.2.1 General**

Slow-front overvoltages on the AC bus of an LCC HVDC converter station, can be caused by switching on transformers, reactors, static var compensators, AC filters and capacitor banks connected to the converter AC bus, and by fault initiation and fault clearing as well as by closing and reclosing of lines. Slow-front overvoltages occur with high amplitude only for the first half cycle of the transient with significantly reducing amplitudes for subsequent cycles. Slow-front overvoltages which originate at locations in the AC network remote from the LCC HVDC converter station usually have magnitudes which are relatively low in comparison with those caused by events occurring close to the converter AC bus.

During the operating life of the equipment, switching of equipment connected to the converter AC bus can occur many times. The overvoltages caused by these routine switching operations are generally less severe than the slow-front overvoltages caused by faults. However, the switching-off of a circuit breaker can, in rare cases, produce a restrike phenomenon and this gives rise to overvoltage.

The selection of AC arresters for LCC HVDC converter stations should consider the presence of existing arresters connected in parallel in the AC network in order to prevent the existing arresters from being overloaded during slow-front and temporary overvoltages.

##### **5.5.2.2 Overvoltages due to switching operations**

Because of the frequency of these operations, it is generally desirable that the surge arresters used to protect equipment do not absorb appreciable energy during these events. Hence, in some cases, the slow-front overvoltages arising from such routine operations are minimized by the use of circuit breakers incorporating closing and/or opening resistors, or by synchronizing the closing and/or opening of the circuit breaker poles, or equipping the breaker with arresters across the poles. The LCC HVDC control system can also be used to effectively damp certain overvoltages such as temporary overvoltages.

Energization of transformers causes inrush current, due to saturation effects, containing harmonics dominated by second order harmonics and other low order harmonics. If one or more of these harmonic currents meet resonant condition, in a network with low damping, high harmonic voltages are produced in the network leading to overvoltage. In an LCC HVDC converter station, resonant conditions are often more severe because of the presence of AC filters and capacitor banks. These capacitances lower the resonance frequency and second or third harmonic resonances can be present.

The temporary overvoltages can last for several seconds, or in rare cases up to a minute.

### **5.5.2.3 Overvoltages due to faults**

When an asymmetric fault occurs in the AC network, transient and temporary overvoltages occur on the healthy phases, influenced by the zero sequence network. In solidly earthed systems that are typical for networks connected to LCC HVDC converter stations, the transient overvoltages (phase-to-earth) normally range from 1,4 p.u. to 1,7 p.u. and the temporary overvoltage from 1,2 p.u. to 1,4 p.u.

Symmetric as well as asymmetric faults could result in transformer saturation. The influence of transformer saturation on overvoltages depends on the instant of fault inception as well as fault clearance. It is therefore necessary to vary the fault conditions when this phenomenon is studied. This fault case is discussed further in Clause 6.

The highest temporary overvoltages most likely occur in conjunction with sudden three-phase faults and complete load rejection if the converters block at the same time as a consequence of the fault without simultaneous disconnection of the filters. The filters and capacitor banks together with the AC system can result in low resonance frequencies. The temporary overvoltages due to faults can be more severe both from the overvoltage point of view and with regard to possible arrester energy stresses. The presence of filters tuned or damped at frequencies between the second and the fifth harmonic can often be effective in reducing the distortion of the voltage and thereby the stresses on the arresters. AC active filters can also be used for this purpose.

### **5.5.3 Slow-front overvoltages on the DC side**

Except for the AC side overvoltages transmitted through the converter transformers, the DC side insulation co-ordination for slow-front overvoltages and temporary overvoltages is mainly determined by fault generated slow-front overvoltages on the DC side.

Events to be considered include DC line-to-earth faults, DC side switching operations, events resulting in an open earth electrode line, generation of superimposed AC voltages due to faults in the converter control (e.g., complete loss of control pulses) misfiring, commutation failures, earth faults and short-circuits within the converter unit. These contingencies are discussed in more detail in Clause 6.

Energization of the DC line with the remote inverter terminal open (rectifier at peak DC output voltage) should also be considered if measures have not been taken to avoid such an event.

In LCC HVDC converter stations with series or parallel connected converter bridge units, events such as a bypass operation on one converter while the second converter bridge unit is in operation shall be considered, particularly during inverter operation.

## **5.6 Fast-front, very-fast-front and steep-front overvoltages**

The different sections of LCC HVDC converter stations should be examined in different ways for fast-front and steep-front overvoltages. The sections include:

- AC switchyard section from the AC line entrance up to the line side terminals of the coverter transformers;

- DC switchyard section from the line entrance up to the line side terminal of the smoothing reactor;
- converter bridge section between the valve side terminal of the converter transformers and the valve side terminal of the smoothing reactor.

The converter bridge section is separated from the other two sections by series reactances, i.e., at the one end, the inductance of the smoothing reactor and at the other end, the leakage reactance of the converter transformers. Travelling waves such as those caused by lightning strokes on the AC side of the transformer on the DC line beyond the smoothing reactor, are attenuated (but can be capacitively transferred as discussed in 6.3.5.4) due to the combination of series reactance and shunt capacitance to earth to a shape similar to slow-front overvoltages. Consequently, they should be considered as part of the slow-front overvoltage co-ordination.

The AC and DC switchyard sections have low impedance compared with overhead lines due to the presence of filters and possibly shunt capacitor banks. The differences from most conventional AC switchyards are the presence of AC filters, DC filters and possibly large shunt capacitor banks, all of which can have an attenuating effect on the incoming overvoltages.

Steep-front overvoltages caused by earth faults in the LCC HVDC converter station, including locations inside the valve hall, are important for insulation co-ordination, especially for the valves. These overvoltages typically have a front time of the order 0,5  $\mu$ s to 1,0  $\mu$ s and durations up to 10  $\mu$ s. The values and waveshapes to be specified should be determined by digital simulation studies, both peak magnitude and maximum rate of change of voltage can be important.

In the AC switchyard section, very-fast-front overvoltages with front times of 5 ns to 150 ns can also be initiated by operation of disconnectors or circuit breakers in gas-insulated switchgear (GIS).

## 6 Arrester characteristics and stresses

### 6.1 Arrester characteristics

Since the late 1970s, overvoltage protection of HVDC converter stations has been based exclusively on metal-oxide surge arresters. This is largely due to their superior protection characteristics compared with the gapped silicon carbide arresters (earlier technology) and their reliable performance when connected in series or parallel with other arresters. The actual arrangement of the arresters depends on the configuration of the HVDC converter station and the type of transmission circuit. The basic criteria used however is that each voltage level and the equipment connected to it is adequately protected at a cost commensurate with the desired reliability and equipment withstand capability.

Metal-oxide surge arresters without gaps are used for the protection of equipment in most modern day HVDC converter stations and are increasingly being used to replace other types of arresters on systems already in service. These arresters provide superior overvoltage protection for equipment compared with gapped silicon carbide arresters due to their low dynamic impedance and high energy absorption capability. The ability of the metal-oxide arrester blocks to share arrester discharge energy when connected in parallel if they are selected to have closely matched characteristics allows any desired discharge energy capability to be realized. Metal-oxide blocks can be connected in several parallel paths within one arrester unit and several arrester units can be connected in parallel to achieve the desired energy capability. Also, parallel connection of metal-oxide blocks can be used to reduce the residual voltage of the arrester, if required.

For metal-oxide arresters, the variation of voltage  $U$  with current  $I$  can be represented by the equation:

$$I = k \cdot U^\alpha$$

where  $k$  is a constant and  $\alpha$  is a non-linearity coefficient of the element material that depends upon the disk formulation and current range being studied. Within the operating range of the arrester the value of this coefficient is high for zinc oxide, typically in the range 10 to 50, as compared to silicon carbide elements used in gapped arresters which exhibit a coefficient of typically 3.

The protective characteristics of an arrester are defined by the residual arrester voltages for maximum steep-front, lightning and switching current impulses that can occur in service. Typical current waveshapes used to define the arrester protective levels are 8/20  $\mu$ s for the LIPL and 30/60  $\mu$ s for the SIPL (IEC 60099-4). The STIPL is usually defined for a current impulse of 1  $\mu$ s front time. The resulting voltage waveforms across the arrester differ because of the high non-linearity coefficient of the arrester block material. The amplitude of the current for which the protective level is specified, which is referred to as the co-ordination current, is usually selected differently for different types of current waveshapes and locations of the arresters. These co-ordination currents are determined from detailed studies carried out during the final stages of the design (see Clause 8).

The arresters used on the AC side are usually specified as for arresters in a normal AC system by their rated voltage and maximum continuous operating voltage. The rated voltage is the maximum permissible r.m.s. value of power frequency voltage between the terminals at which the arrester is designed to operate correctly, as established in the operating duty tests. The maximum continuous operating voltage is used as a dimensioning parameter for the specification of operating characteristics.

For the arresters on the DC side of an LCC HVDC converter station, the continuous operating voltage is defined differently because the voltage waveshape which continuously appears across the arresters consists, in many cases, of superimposed direct, fundamental and harmonic components and, in some cases, also of commutation overshoots. The arrester voltages are specified in terms of peak continuous operating voltage (PCOV), crest value of continuous operating voltage (CCOV), and equivalent continuous operating voltage (ECOV), as defined in Clause 3. This means that the tests specified for these arresters shall be adjusted for the particular applications, different from standard tests usually applicable for AC arresters. The required energy capability of the arresters shall consider the applicable waveshapes as well as the amplitudes, duration and the number of respective discharges. For the filter arrester, the required energy capability shall be considering the dissipation energy due to harmonics.

## **6.2 Arrester specification**

The residual voltage of an arrester is the peak voltage that appears between the terminals of an arrester during passage of a discharge current. The arrester currents for which the maximum residual voltages are specified are called the co-ordination currents as illustrated in Table 5.

The values of co-ordination currents are determined by system studies, usually carried out by the supplier. The process involves taking into account the energy duty in arresters, the number of arrester columns in parallel and the peak current in each arrester which depends on the number of arresters in parallel. The final choice for peak current in the arresters is the co-ordination current for which the corresponding residual voltage leads to the representative overvoltage for directly protected equipment. What is looked for is the "best balance" between overall arrester specifications and design and HVDC converter equipment voltage withstand requirements and design, this process resting on the choice of co-ordination currents.

For arrester testing purposes and protection levels assessment, standard shapes defined in IEC 60099-4 for switching, lightning and steep current impulse are applied to the co-ordination currents.

For the sections of the HVDC converter station exposed to atmospheric overvoltages, the determination of the arrester co-ordination current for lightning stresses shall consider the design of the station shielding (particularly for outdoor valves). The maximum current at shielding failure can be determined, for example, according to *Guide to procedures for estimating the lightning performance of transmission line* (CIGRE), or *Transmission line reference book – 200 kV and above* (EPRI).

Arrester discharge currents during contingencies can be of various durations. In specifying the arrester energy capability, consideration shall be given to both the amplitude and duration of the discharges, including repetitive stresses due to the relevant operating sequence. Repetitive current impulses occurring over several cycles of fundamental frequency are considered as one single discharge, having an equivalent energy content and duration as the accumulated values of the actual energy impulses, and taking into account current amplitudes and durations of the combined impulses. From a thermal stability point of view, repetitive current impulses shall be considered over a longer period of time. When determining the equivalent energy, it shall also be taken into account that the energy withstand capability of metal-oxide arresters is reduced with shorter pulse duration, less than 200  $\mu$ s (*Guidelines for the application of metal-oxide arresters without gaps for HVDC converter stations* [CIGRE]).

In specifying the arrester capability, the calculated arrester energy value from the studies can consider a reasonable safety factor. This safety factor is in the range of 0 % to 20 %, depending on allowances for tolerances in the input data, the model used, and the probability of the decisive fault sequence giving higher stresses than the cases which have been studied.

### 6.3 Arrester stresses

#### 6.3.1 General

A typical arrester arrangement between the AC side of the converter bridges and the DC transmission circuit is shown in Figure 3 for a two-terminal bipolar LCC HVDC scheme with one 12-pulse converter per pole. It should be noted however, that some of the arresters probably not be used, depending upon the overvoltage withstand capability of the equipment connected at that point, and upon the overvoltage protection afforded by a combination of other arresters at the same point. For example, the DC bus can be protected by a series combination of the bridge (B) and mid-point DC bus (M) arresters, instead of the converter unit DC bus arrester (CB).

Similar protective arrangements can be used for stations with two 12-pulse converters per pole or for back-to-back stations. In the latter case, only the valve arresters (V) are normally needed on the valve side since the operating voltage is much lower than for a line or cable transmission scheme. However, mid-point bus (M) or bridge (B) arresters are sometimes included.

For HVDC converter stations connected directly to DC cables, the DC bus/line arresters (DB and DL) can be deleted since the pole probably not be exposed to fast-front overvoltages.

On the AC side of the HVDC converter station, phase-to-earth arresters (A) are normally provided to protect the converter AC bus and the AC filter bus.

Arresters are also normally connected across both AC and DC harmonic filter reactors or from the high-voltage terminals of the filter reactors to earth, as shown in Figure 3.

In systems involving a combination of DC cables and/or overhead lines, arresters can be needed at the cable terminations to protect them from overvoltages originating from the overhead line.

The basic principles when selecting the arrester arrangement are that:

- overvoltages generated on the AC side should, as far as practicable, be limited by arresters on the AC side. The main protection is given by the AC bus arresters (A);

- overvoltages generated on the DC line or earth electrode line should, in a similar way, be limited by DC bus, DC line/cable arresters (DB and DL/DC), converter bus arresters (CB), and neutral bus arresters (E).

For overvoltages within the HVDC converter station, critical components should be directly protected by arresters connected close to the components, such as valve arresters (V) protecting the thyristor valves and AC bus arresters (A) protecting the line side windings of the transformers. Protection of the valve side of the transformers will usually be achieved by arresters connected in series, e.g., a combination of bridge arrester (B), mid-point arrester (M) and a valve arrester (V). However, where the HVDC converter station transformers can be disconnected from the bridges, provision should be made to protect the transformer valve windings.

### **6.3.2 AC bus arrester (A)**

The AC side of an HVDC converter station is protected by arresters at the converter transformers and at other locations depending on the station configuration (see for example Figure 3). These arresters are designed according to the criteria for AC applications and they limit the overvoltages on both the line side and the valve side of the converter transformers, taking into account the overvoltages transferred from the line side to the valve side of the transformers through inductive and stray capacitance coupling.

The large size of reactive sources in the form of shunt capacitors and filter banks tend to limit the duty seen by the arresters due to switching and lightning overvoltages entering from the AC system. However, high energy duty could be imposed due to discharges of the charged shunt reactive banks.

These arresters are designed for the worst case of fault clearing followed by recovery, including transformer saturation overvoltages and overvoltages due to load rejection, as well as possible restrike of circuit breakers during their opening.

Because of possible saturation overvoltages of high amplitude and long duration, this arrester probably needs to be designed for high energy duty.

Care should be taken to coordinate the A arresters with any already existing AC arresters at or near the commutating bus. Depending on the station layout long separation distances can dictate the use of AC bus arresters at several locations.

If these arresters are used to limit temporary overvoltages, especially during load rejection at weak AC system conditions under possible low order resonance conditions, they would be subjected to high energy duty requiring multiple columns.

### **6.3.3 AC filter arrester (FA)**

The AC filter reactors and resistors can be protected by AC filter arresters.

The continuous operating voltage of the AC filter arrester consists of a power frequency voltage with superimposed harmonic voltages corresponding to the resonance frequencies of the filter branch. The ratings of these arresters are normally determined by the transient events. Since the harmonic voltages result in relatively high power losses in the arrester, these shall also be considered in the rating of arresters.

The events to be considered with respect to filter arrester duties are slow-front plus temporary overvoltages on the AC bus and discharge of the filter capacitors during earth faults on the filter bus. The former determines the required SIPL and the latter the LIPL and the energy discharge requirement. In certain cases, high energy discharge duties can also result from conditions of low order harmonic resonance or possibly due to low order non-characteristic harmonics generated by unbalanced operation during AC systems faults.



The arrester energy duties shall be the highest of the following duties:

- a) Filter capacitors are charged to the maximum fundamental frequency phase-to-earth voltage.
- b) The AC bus is charged to the switching surge protective level, prior to fault application.
- c) Temporary overvoltages, especially during load rejection at weak AC system conditions under possible low order resonance conditions, especially for low-order harmonic filters.

#### 6.3.4 Transformer valve winding arresters (T)

The valve arresters in combination with other arresters typically provide protection to transformer valve windings. In general phase-earth arresters on the valve side of the converter transformer (T) are not provided for LCC HVDC schemes up to 600 kV.

However, at higher voltages (800 kV and above), phase-earth arresters connected to the valve winding of the top 6-pulse transformer can be considered with a view to reduce the phase-earth insulation level of the valve winding of the top 6-pulse transformer.

#### 6.3.5 Valve arrester (V)

##### 6.3.5.1 General

Valve arresters (V) are installed, close to the valves, in parallel with each valve.

The main purpose of the valve arrester is to protect the thyristor valves from excessive overvoltages. This arrester and/or the protective firing of thyristors in the forward direction constitute the overvoltage protection of the valve. Since the cost of the valves and also their power losses are roughly directly proportional to the insulation level across the valves, it is essential to keep this insulation level and therefore the arrester protective level as low as possible.

##### 6.3.5.2 Continuous operating voltage

The valve arrester continuous operating voltage consists of sine wave sections with commutation overshoots and notches as shown in Figure 5. Disregarding the commutation overshoots, the crest value of the continuous operating voltage is proportional to  $U_{di0max}$  and, as per 5.2, it is given by the following formula:

$$U_{ccov} = \frac{\pi}{3} \cdot U_{di0max} = \sqrt{2} \cdot U_{v0}$$

The peak continuous operating voltage (PCOV), which includes the commutation overshoot, shall be considered when the reference voltage of the arrester is determined. The commutation overshoot is dependent on the firing angle  $\alpha$  and the maximum value can occur when the valve operates with large firing angles.

For normal firing angles (alpha and gamma) typical values of commutation overshoot range between 15 % to 25 % of the CCOV for a duration of 100  $\mu$ s to 300  $\mu$ s.

##### 6.3.5.3 Temporary and slow-front overvoltages

###### 6.3.5.3.1 General

The maximum temporary overvoltages are transferred from the AC side, normally, during fault clearances combined with load rejections close to the HVDC converter station. However, it shall be noted that only contingencies without blocking, or with partial blocking of the converters need to be considered, since the valve arresters are relieved from stress when the valve is blocked and the by-pass pair is extinguished.

The events producing significant valve arrester -currents of switching character are as follows:

- a) earth fault between the converter transformer and the valve in the commutating group at highest potential;
- b) clearing of an AC fault close to the HVDC converter station;
- c) current extinction in only one commutating group (if applicable).

#### **6.3.5.3.2 Earth fault between the converter transformer and the valve**

A phase-to-earth fault on the valve side of the converter transformer of the bridge at the highest DC potential will give significant stresses on the valve arresters in the upper commutation group. The discharges through the arresters are composed in principle of two current peaks. Firstly, the stray and the damping capacitances of the converter are discharged giving steep-front surge stresses on the valve connected to the faulty phase (see 6.3.5.4). Secondly, the DC pole and line/cable capacitances are discharged through the DC reactor and the transformer leakage reactance giving a slow-front overvoltage type, approximately 1 ms to crest. This latter discharge might expose one of the arresters connected to the other phases with the highest current and energy. The parameters such as the DC voltage at the fault instant, DC reactor inductance, transformer leakage inductance and line/cable parameters determine which of the three upper arresters will be the most stressed and the magnitude of these stresses. For DC schemes having parallel connected converters, this phase to earth fault case implies additional stresses since the unfaulted converter will continue to feed current into the earth fault for some time before the protection trips the converters. Depending on current rating, control system dynamics, inductance of the DC reactor, and the protection scheme, this phase-to-earth fault case can be dimensioning for the energy and current rating of the arresters across the upper three valves.

In the above phase-to-earth fault case, the calculated stresses are highly dependent on the value of the DC bus voltage. It is recommended using the maximum DC voltage that can last for a number of seconds. It should be noted that this case can lead to an arrester with very high energy discharge capability. The final decision should consider the probability for the occurrence of voltage higher than the maximum operating voltage in combination with an earth fault.

#### **6.3.5.3.3 Fault clearance**

At fault clearing in the AC network, excessive overvoltages on the AC side arise only if the converters are blocked. If the converters continue to operate after the fault, this will damp out the overvoltages and the total discharge energy will be much smaller. Often the case that gives the maximum arrester energy is when the converter is permanently blocked with by-pass pairs. The blocking might imply that the converter transformer breakers are opened a few cycles later. If this is the case, the arresters are not exposed to any operating voltage after the fault is cleared. A realistic tap changer position for a relevant load flow shall be used when the transferred overvoltages from the line side are calculated. Unfavourable system conditions can result in ferroresonance between the AC filter/shunt capacitor and the converter transformer together with the AC network impedance. The fault inception and the instant of fault clearance instants should be varied in order to cover the variations in transformer saturation.

#### **6.3.5.3.4 Current extinction**

A current extinction in all three valves of one commutating group, while the valves in the commutating groups in series still conduct current, might be decisive for the arrester energy rating. The current is then forced to commute to one of the arresters connected in parallel with the non-conducting valves. The energy dissipated in this arrester can be substantial if the current is not quickly reduced to zero.

Possible contingencies which can result in current extinction in the valves in only one commutating group include:

- a) firing failure in a valve, e.g., due to a failure in the valve control unit;

- b) blocking of all the valves in a converter without firing of the by-pass pairs. This contingency can give a converter current close to zero, during some transient conditions such that the current is only extinguished in one of the commutating groups connected in series. This case is often most stringent during inverter operation.

If current extinction is considered inconceivable then this event is excluded. Whether the current extinction is conceivable or not depends very much on the degree of redundancy and type of control/protection system.

#### **6.3.5.4 Fast-front and steep-front overvoltages**

The valves and the valve arresters within the converter area are separated from the AC switchyard and the DC switchyard by large series reactances, i.e., the converter transformers and the smoothing reactors. Travelling waves, caused by lightning strokes on the AC side of the transformers or on the DC line outside of the smoothing reactor, are attenuated by the combination of series reactances and earth capacitances to a smaller magnitude or a shape similar to slow-front overvoltages. However, in the case of large transformer ratios (e.g., back-to-back stations) the capacitive coupling is more predominant and can need consideration. The valve and valve arresters can in general only be subject to fast-front and steep-fronted overvoltages at back-flashovers and earth faults within the converter area. Direct lightning strokes shall be considered only if the lightning passes the shielding system. Direct strokes and back-flashovers can often be excluded in high-voltage HVDC converter stations with adequate shielding and earthing systems.

The most critical case for steep-front overvoltages is normally an earth fault on the valve side of the converter transformer of the bridge with the highest DC potential. The circuit is modelled in detail with its stray capacitances and bus inductances represented for the estimation of this case.

A contingency to be recognized in the design of the thyristor valve is when the valve is stressed by a forward overvoltage and the valve is fired during the overvoltage resulting in the immediate commutation of the arrester current from the arrester to the valve. It should be stressed that the arrester current to be considered for this commutation is not necessarily the specified co-ordination current for the valve arrester, which normally refers to an overvoltage in the reversed direction. For an overvoltage in the forward direction, it is adequate to assume a co-ordination current of switching character corresponding to the protective firing level across the valve. However, the tolerances in the arrester characteristics and redundant thyristors can be considered when the arrester current is estimated.

#### **6.3.5.5 Valve protective firing (PF)**

Valve protective firing can limit overvoltage across the valve by triggering the thyristors. There are two different strategies used to co-ordinate the protective firing level with the protective level of the valve arrester.

In the first strategy, the overvoltage protection between valve terminals in both the reverse and the forward direction is afforded by the valve arrester, and the thyristor firing threshold is set higher than the protective level of the valve arrester. In this strategy, valve protective firing action is used to protect the individual thyristor levels in the event of loss of firing signals, severe non-linear voltage distribution under fast transient or steep-front voltages within the valve.

In the second strategy, while the valve arrester limits overvoltages in the reverse direction, protective firing threshold in the forward direction for the valve is set lower, typically at 95% to 98 % of the valve arrester protective level, thus providing the main overvoltage protection in the forward direction. However, the second strategy can be used only when the reverse withstand voltage of the thyristor is higher than the forward withstand voltage of the thyristor. This approach would normally lead to fewer thyristor levels in a valve than with the first strategy, resulting in reduced costs and improved converter efficiency. The protective firing threshold should be set sufficiently high to ensure that activation of protective firing is avoided during the highest temporary overvoltages (taking into account commutation transients and voltage imbalance) or during events which occur frequently (e.g., switching operations). This is to minimize undue interruption of power transmission and facilitate speedy recovery following faults which occur with the converter remaining in operation.

The level of the protective firing shall be co-ordinated with the overvoltages during different operating conditions. The level of protective firing and arrester protective levels should be stated as part of the valve design. Possible adverse effects of the protective firing on the transmission performance need only be considered during external faults when the pole remains in operation and then, in particular, during inverter operation.

Valve protective firing in rectifier operation during transients in the AC network does not give rise to any significant disturbance of the link. On the other hand, if a valve is fired earlier due to a protective firing during inverter operation, the result could be a commutation failure and the recovery time for the transmission after a fault clearing can be increased. In order not to affect the recovery of the link, the valve protective firing should not be activated during the highest overvoltage that can occur without permanent blocking of the converter acting as inverter.

#### **6.3.6 Bridge arrester (B)**

A bridge arrester can be connected between the DC terminals of a six-pulse bridge. The bridge arresters can be provided across the lower six-pulse bridge and/or the upper six-pulse bridge. The upper bridge arrester along with the mid-point arrester provides protection for the DC bus to earth.

Disregarding the commutation overshoots, the crest value of the continuous operating voltage (CCOV) is the same as for the valve arrester, described in 6.3.5.2. The peak continuous operating voltage (PCOV), which includes the commutation overshoot, shall be considered when the reference voltage of the arrester is determined. The commutation overshoot is dependent on the firing angle  $\alpha$  and the maximum value can occur when the valve operates with large firing angles.

The following events can produce arrester currents of switching impulse type:

- a) clearing of an AC fault close to the HVDC converter station;
- b) current extinction in the corresponding six-pulse bridge (if applicable, see 6.3.5.3.4).

The switching overvoltages transferred from the AC side normally result in low arrester currents since the bridge arrester is then connected in parallel with a valve arrester.

#### **6.3.7 Converter unit arrester (C)**

A converter unit arrester can be connected between the DC terminals of a 12-pulse converter, arrester C in Figure 3.

The maximum operating voltage is composed of the maximum direct voltage from one converter unit plus the 12-pulse ripple.

The theoretical maximum operating voltage for zero values of the firing delay and overlap angles is given by the following expression:

$$U_{\text{ccov}} = 2 \cdot U_{\text{di0max}} \cdot \frac{\pi}{3} \cdot \cos(15^\circ)$$

In practice the CCOV is smaller and can be estimated during the preliminary design stage using the following equation:

$$U_{\text{ccov}} = 2 \cdot U_{\text{di0max}} \cdot \frac{\pi}{3} \cdot \cos^2(15^\circ)$$

Digital simulations can be used to determine the CCOV under possible steady state operating conditions.

The commutation overshoots should be considered in the same way as for the valve arrester when the arrester is specified.

The converter unit arresters are normally not exposed to high discharge currents of switching character. For series connected converters, the formation of a by-pass pair during blocking of a valve group or accidental closing of the by-pass switch will stress this arrester. The arrester can limit overvoltages due to lightning stresses propagating into the valve area, although these stresses are not decisive for the arrester.

### 6.3.8 Mid-point DC bus arrester (M)

A mid-point DC bus arrester is sometimes provided to reduce the insulation level of the upper converter transformers of a 12-pulse converter. The mid-point arrester can be connected from the mid-point of a 12-pulse converter to earth (arrester M in Figure 3, MH and ML in Figure 1).

The mid-point arrester CCOV is equal to the valve arrester CCOV plus an offset due to the voltage drop in the return path, for the case of inverter operation. The commutation overshoots should be considered in the same way as for the valve arrester when this arrester is specified.

An event producing significant arrester stresses of switching character, when applicable (see 6.3.5.3 above), is current extinction in the lower six-pulse bridge. Also, operation of by-pass switches will give rise to stresses, in the case of series connected converter units. Lightning stresses can result from shielding failures.

### 6.3.9 Converter unit DC bus arrester (CB)

A converter unit DC bus arrester can be connected between the bus and earth (arrester CB in Figure 3), to protect the equipment, connected to the high voltage DC pole, on the converter side of the smoothing reactor.

The operating voltage is similar to that for the converter unit arrester with the addition of the voltage drop in the earth electrode line, for the case of inverter operation.

Due to the high protective level, the arrester will normally not be exposed to high discharge current from slow-front overvoltages. Lightning stresses of moderate amplitude can result from shielding failures.

### 6.3.10 DC bus and DC line/cable arrester (DB and DL/DC)

The DC bus arrester DB is used to protect the DC switchyard equipment connected to the DC pole. Usually, separation distance considerations can dictate installation of arresters at more than one location to provide adequate protection to different parts of the station. If more than one arrester is provided, the arrester on the line (cable) entrance is designated as DC line (DC cable) arrester DL (DC). When the LCC HVDC transmission comprises overhead line sections as well as cable sections, consideration should be given to the application of surge arrester DC at the cable-overhead line junction to prevent excessive overvoltages on the cable.

For HVDC converter stations where the DC cable is connected directly to the converter indoor bus, the DC bus/cable arrester (DB and DC) cannot be used since the pole probably is not exposed to fast-front overvoltages.

The maximum operating voltage is almost a pure DC voltage with a magnitude dependent on the converter and tap-changer control and possible measurement errors.

These arresters are mainly subjected to lightning stresses. Critical slow-front overvoltages can often be avoided by suitable selection of the parameters in the main circuit, thus avoiding critical resonances. A pole to earth fault in one pole of a bipolar overhead DC line will produce an induced overvoltage on the healthy pole. The magnitude of these overvoltages is dependent on the location of the fault, the line length and the termination impedance of the line. Normally, these types of overvoltages are not critical for the insulation of the terminals.

For faults at the cable junction, high switching surge type overvoltages could occur at the converter terminal on the opposite side of the faulted side, if the length of the cable is short.

In the case of LCC HVDC transmission system with long cables, the energy rating of the cable arresters is decided by the discharge of the cable from the highest voltage it can attain during a contingency. This normally results in comparably low discharge currents, but possibly high energy discharge through the arresters. Contingencies to be considered are valve misfire and complete loss of firing pulses in one of the stations, starting the rectifier against open or blocked inverter.

For a line/cable junction the lightning stresses on the cable arresters DC are not significant due to low surge-impedance of the cable, if the overhead line is effectively shielded and towers are provided with low footing resistance values for at least a few spans from the junction.

### 6.3.11 Neutral bus arrester (E, EL, EM in Figure 3, EB, E1, EL, EM in Figure 1)

The neutral bus arrester protects the neutral bus and the equipment connected to it. In combination with valve arrester(s) it can also protect the bottom converter transformer(s). The separation distance between the arresters and the point of protection can dictate the installation of arresters at more than one location to give adequate protection to different parts of the station.

The normal operating voltage of the arrester EB (with a smoothing reactor on the neutral line), would consist of ripple voltages and could be substantial.

For the rest of the neutral bus arresters E1, EL, EM the operating voltages are normally low. At balanced bipolar operation they will be practically zero.

However, during monopolar or metallic return operation the operating voltage on all these arresters EB, E1, EL and EM increase by the DC offset.

These arresters are provided to protect equipment from fast-front overvoltages entering the neutral bus and from the overvoltages described below.

These arresters should be designed to discharge large energies during an earth fault on the DC bus or DC line and an earth fault between the valves and the converter transformer. In the event of loss of return path during monopolar operation it could result in an excessive energy rating, and a sacrificial arrester can be a preferred choice under this event. An earth fault on the DC bus can cause the DC filter to discharge through the neutral bus arrester, giving a very high but short current peak, depending upon the DC filter and DC filter arrester configuration. The most essential assumption is the pre-fault voltage of the filter which normally is chosen as the maximum operating DC voltage. The fast discharge of the DC filter is followed by a slower fault current from the converter. The rate of rise is mainly limited by the DC reactor. The fault current will be shared between the earth electrode line and the neutral bus arrester. In the case of metallic return operation, the impedance in parallel with the arrester is the entire DC line impedance.

At an earth fault on a phase between the valve and the converter transformer, the AC driving voltage will be shared between the converter transformer impedance and the earth electrode line impedance. The decisive case can be found for the terminal which has the longest earth electrode line and, in the case of metallic return operation, in the unearthed terminal. The worst case occurs when the station is operating as rectifier, because of the polarity of the driving voltage.

A metallic return operation usually gives such high requirements on the neutral bus arrester, that it becomes advantageous to select a higher arrester rating in the unearthed station than in the station that is earthed during metallic return operation. This is also applicable for long electrode lines (normally for distances above 50 km).

Neutral bus capacitors have been included in recent schemes, mainly due to harmonic filtering requirements and due to suppression of overvoltages on the neutral bus, although they will influence the neutral bus arrester stresses and shall be included in the study model. The stresses on the neutral bus arrester will also depend on the converter control and protective actions taken during the fault.

When the energy rating results in an excessive design, under unlikely events, a sacrificial arrester can be considered. In particular, this is the preferred design when the replacement of the arrester does not significantly influence the outage time. In bipolar systems sacrificial arresters shall be located so that bipolar outages are avoided.

If a smoothing reactor is provided in the neutral bus special care should be taken in the co-ordination (reference voltages and energy requirements) of the neutral arresters (EB, E1, EM, EL). If a neutral blocking filter is provided it should be also considered for the arrester co-ordination.

### **6.3.12 DC reactor arrester (DR)**

The DR arrester provides terminal-to-terminal protection for the smoothing reactor.

The smoothing reactor acts as a buffer between the DC line and the converter station for lightning surges entering from the DC pole. It is desirable to keep the arrester protective level/smoothing reactor insulation level as high as possible in order not to sacrifice this buffer effect.

The operating voltage of the smoothing reactor arrester consists only of a small 12-pulse ripple voltage from the converter.

The arrester will be subjected to lightning overvoltages of opposite polarity to the converter DC bus operating voltage (which can be termed subtractive lightning impulses). The possibility of lightning stresses being coupled through the arrester to the thyristor bridge shall be considered.

In many schemes the smoothing reactor arrester can be dispensed with when the reactor insulation level meets the voltage requirement from the DC line arrester combined with the maximum operating voltage of opposite polarity.

### **6.3.13 DC filter arrester (FD)**

The DC filter reactors and resistors are protected by the DC filter arresters FD.

The normal operating voltage of the DC filter reactor arrester is low and usually consists of one or more harmonic voltages corresponding to the resonance frequency of the filter branch in question. Since the harmonic voltages result in relatively high power losses these shall be considered in the rating of arresters.

Arrester duties are mainly determined by filter capacitor discharge transients resulting from earth faults on the DC pole, and occasionally due to lightning surges.

### **6.3.14 Earth electrode station arrester**

The equipment at the earth electrode station, for example distribution switches, cables and measuring equipment, requires protection from overvoltages entering via the earth electrode line. An arrester can be installed at the line entrance. The continuous operating voltage is insignificant. The arrester is dimensioned for lightning stresses entering via the overhead line.

## **6.4 Protection strategy**

### **6.4.1 General**

Because of the nature of the HVDC configurations some of the equipment/points are directly protected by a single arrester connected across their terminals while some others are protected by a series combination of more than one arrester.

### **6.4.2 Insulation directly protected by a single arrester**

The maximum overvoltage between points directly protected by their own single arresters (for example valve arrester V across points 5 to 9 in Figure 3) is determined from the arrester characteristics together with the co-ordination current through the arrester. Some of the points that can be protected by a single arrester are listed below:

- a) thyristor valve;
- b) converter terminals;
- c) DC mid-point bus;
- d) converter transformer valve winding phase-to-earth (especially the upper six-pulse bridge);
- e) neutral bus;
- f) smoothing reactor;
- g) DC filter components;
- h) line side of DC bus;
- i) valve side of DC bus;
- j) AC bus;
- k) AC filter components.

### **6.4.3 Insulation protected by more than one arrester in series**

For insulation not directly protected by a single arrester, the protection can be achieved by a number of arresters connected in series as shown in Table 2 and Table 3.



In this case the protective level of the insulation is defined by the sum of the voltages of the individual arresters, during the decisive event. It is to be noted that this can not necessarily be the sum of the protective levels of the individual arresters.

#### **6.4.4 Valve side neutral point of transformers**

For slow-front overvoltages and temporary overvoltages, the maximum voltage in the neutral is the same as the phase-to-earth voltage on the corresponding AC phase as shown in Table 2 and Table 3.

#### **6.4.5 Insulation between phase conductors of the converter transformer**

Slow-front overvoltages can occur between the phases on the line side and the valve side of the converter transformers, stressing the air clearance between conductors in the switchyard. Usually, this is not a problem for the lower system voltage, but in the case of high AC system voltages and a number of series connected valve bridges, the maximum voltage shall be evaluated and air clearances between conductors in the switchyard designed accordingly.

The inter-winding voltages can stress different points inside the converter transformer depending on its construction (two-or three winding, single-or three-phase transformer).

When the valves in a valve bridge are conducting, the phase-to-phase insulation is protected by one valve arrester V. When the valves are not conducting the phase-to-phase insulation is protected by the AC bus arresters A transferred to the valve side.

#### **6.4.6 Summary of protection strategy**

Table 2 and Table 3 are a summary of the arrester protections for different points on the DC side, based on the examples of Figure 1 and Figure 3 respectively. Such tables should be established in light of the specific design.

The tables assume that the converters are deblocked and that at each 3-pulse level there is at least one conducting valve. In that way, the protective level across each 6-pulse bridge is the voltage across one conducting valve and the voltage across one valve arrester, i.e., the protective level across the 6-pulse bridge will be V.

When the valves are not conducting, there are 2 cases to consider:

- Lightning surges coming from DC or AC sides are attenuated both in amplitude and slope as they only can penetrate through the DC pole reactor stray capacitances or through the converter transformer inter-winding capacitance. They will be distributed by the capacitances in the circuit, and the stresses will be lower than for the case with deblocked converters.
- Switching surges coming from the AC side are phase-to-phase voltages. As the valves are blocked there is no connection to earth and therefore the only overvoltage possible is the transferred phase-to-phase voltage, limited by the AC bus arresters in the primary side. Switching surges coming from the DC side will be distributed by the impedance of the blocked valves, and the stresses will be lower than for the case with deblocked converters.

**Table 2 – Arrester protection on the DC side: one 12-pulse converter (Figure 3)**

Protected item	Protecting arrester(s)	Comments
Between terminals of a valve	V	
Between terminals of a 6-pulse bridge	(1) V (2) B	
Between terminals of the 12-pulse group	(1) C (2) 2·V	
Between terminals of smoothing reactor	DR	Can be omitted
DC bus line side of smoothing reactor	DB, DL/DC	
DC bus, valve side of smoothing reactor	(1) CB (2) C + E (3) B + M (4) 2·V + E	
Mid-point DC bus	(1) M (2) V + E	
Neutral bus	E, EL, EM	
HV transformer, phase to earth	(1) T (2) V + M (3) 2·V + E	
LV transformer, phase to earth	V + E	
HV and LV transformers, phase to phase	Arrester A protective level transferred to the valve side	
NOTE The numbers () above refer to possible alternatives. The minimum alternative can be selected.		

**Table 3 – Arrester protection on the DC side: two 12-pulse converters in series (Figure 1)**

Protected item	Protecting arrester(s)	Comments
Between terminals of a valve	V	
Between terminals of a 6-pulse bridge	(1) V (2) B	
Between terminals of a 12-pulse group	(1) CH, CL (2) 2·V	
Between terminals of the 2x12-pulse group	(1) CB + EB (2) CH + CL (3) 4·V	
Between terminals of HV smoothing reactor	DR	Can be omitted
Between terminals of LV smoothing reactor	EB + E1	Very conservative assumption. Can be reduced
DC bus, line side of HV smoothing reactor	DB, DL/DC	
DC bus, valve side of smoothing reactor	(1) CB (2) CH + CM (3) 2·V + CM (4) 4·V + E	
Mid-point between 6-pulse bridges of the HV 12-pulse group	(1) MH (2) V + CM	
Mid-point DC bus	(1) M (2) 2·V + E	
Mid-point between 6-pulse bridges of the LV 12-pulse group	(1) ML (2) V + EB	
Neutral bus, valve side of LV smoothing reactor		
Neutral bus, line side of LV smoothing reactor	E1, EL, EM	
HV transformer, HV 12-pulse group, phase to earth	(1) T (2) V + MH	
LV transformer, HV, 12-pulse group, phase to earth	V + CM	
HV transformer, LV 12-pulse group, phase to earth	(1) V + ML (2) 2·V + EB	
LV transformer, LV 12-pulse group, phase to earth	V + EB	
HV and LV transformers, HV and LV 12-pulse groups, phase to phase	Arrester A protective level transferred to the valve side	
NOTE The numbers () above refer to possible alternatives. The minimum alternative can be selected.		

### 6.5 Summary of events and stresses

In Clauses 5 and 6, a description is provided about the expected continuous, temporary, slow-front, fast-front and steep-front stresses that the equipment and arresters would be exposed to in an LCC HVDC converter station.

These events and stresses are summarized in Table 4 and Table 5.

Table 4 relates to various contingencies and the affected arresters. Table 5 gives information concerning the type of stresses the different arrester experience, and whether the current or energy stresses can be of significance for particular contingencies and arresters. This information can be used to decide on the relevant system model for detailed studies.

**Table 4 – Events stressing arresters: one 12-pulse converter (Figure 3)**

Event	Arresters (refer to Figure 3 for arrester designation)											
	FA	A	T	V B	M	CB C	E	EL	EM	DR	DB DL DC	FD
Earth fault, DC pole or DC line (nodes 9, 10, line 1)			x				x	x	x	x	x	x
Lightning from DC line							x		x	x	x	x
Slow-front overvoltages from DC line							x	x	x		x	x
Lightning from earth electrode line							x	x				
Earth fault AC-phase on valve side (nodes 5, 6)				x	x		x	x	x	x		
Current extinction three-pulse commutation group				x								
Current extinction six-pulse bridge				x	x							
Loss of return path, monopolar operation or commutation failure							x	x	x			
Earth faults and switching operation, AC side	x	x	x	x	x	x	x	x	x	x		x
Lightning from AC system	x	x										
Station shielding failure, pole bus (at nodes 9, 10, if applicable)				x	x	x						
Station shielding failure, neutral bus (at node 8, if applicable)							x	x	x			
Some events may not need to be considered due to a too low probability occurrence.												

**Table 5 – Types of arrester stresses for different events:  
one 12-pulse converter (Figure 3)**

Event	Fast-front and steep-front stresses		Slow-front and temporary overvoltage stresses	
	Current	Energy	Current	Energy
Earth fault, DC pole or DC line (nodes 9, 10, line 1)	E, EL, EM, FD	E, EL, EM, FD	DB, DL/DC, DR, E, EL, EM, T	E, EL, EM
Lightning from DC line	DB, DL/DC, FD DR, E, EM			
Slow-front overvoltages from DC line			DB, DL/DC, E, EL, EM, FD	
Lightning from earth electrode line	E, EL			
Earth fault on bridge AC phase (nodes 5, 6)	V, B		DR, V, B, E, EL, EM, M	V, B, E, EL, EM, M
Current extinction, three-pulse group			V, B	V, B
Current extinction, six-pulse group			M, V, B	M, V, B
Loss of return path, monopolar operation or commutation failure			E, EL, EM	E, EL, EM
Earth faults and switching operations on AC side (node 1, AC line)	FA	FA	V, M, CB, A, FA E, EL, EM, FD, DR, C, B, T	V, B, A, E, EL, EM, FD
Lightning from AC system	A, FA			
Station shielding failure, pole bus (at nodes 9, 10, if applicable)	V, M, CB, C, B			
Station shielding failure, pole bus (at nodes 8, if applicable)	E, EL, EM			
Some events may not need to be considered due to a too low probability of occurrence.				

Converter contingencies such as commutation failures or inverter blocking without by-pass pairs are not critical for determining protective levels and energy requirements of the LCC HVDC converter station arresters. However, inverter blocking with current can be important for determining arrester energy requirements, unless if considered inconceivable (6.3.5.3.4). Some cases of commutation failures can be critical (e.g., giving rise to resonances, or in a situation involving the combination of the low neutral arrester protective level (E, EL, EM) and high impedance of a DC current return path).

## 7 Design procedure of insulation co-ordination

### 7.1 General

The principles of insulation co-ordination are described in IEC 60071-11:–, Clause 5.

The LCC HVDC insulation co-ordination procedure is recommended in IEC 60071-11:–, Clause 6. The studies are generally, but not necessarily, based on assessment and evaluation of various transient events affecting the stresses on different arresters using the methods and tools such as those discussed in Clause 8.

Subclauses 7.2 to 7.6 suggest some illustrative tables suitable both for itemizing the quantities which are to be the design objectives in a clear manner and as a possible means of presenting the design results.

## 7.2 Arrester requirements

Table 6 suggests for each of the arresters, such as referenced in Figure 3, the various requirements which should be the objectives of the insulation co-ordination design. The suggested (or similar) format on groups of arresters and individual items, should facilitate clear identification and presentation of the information.

**Table 6 – Arrester requirements**

Arrester identification – reference <sup>a, b</sup>	Continuous operating voltages			Arrester protective levels at co-ordination currents <sup>a</sup>						Energy absorption
	$U_c, U_{ch}$	CCOV	PCOV	SIPL		LIPL		STIPL <sup>c</sup>		Duty of arrester
(See Figure 1 and Figure 3)	kV (r.m.s.)	kV (crest)	kV (peak)	kV (peak)	kA (peak)	kV (peak)	kA (peak)	kV (peak)	kA (peak)	kJ
<b>I. AC section</b>										
<b>A</b>		N/A	N/A					N/A	N/A	
<b>FA1, FA2</b>		N/A	N/A					N/A	N/A	
<b>II. Converter circuit</b>										
<b>V</b>	N/A									
<b>T</b>	N/A							N/A	N/A	
<b>B</b>	N/A							N/A	N/A	
<b>M, MH, ML</b>	N/A							N/A	N/A	
<b>C, CH, CL, CB</b>	N/A							N/A	N/A	
<b>III. DC yard</b>										
<b>DB, DL, DC</b>	N/A		N/A					N/A	N/A	
<b>EB</b>								N/A	N/A	
<b>DR</b>		N/A						N/A	N/A	
<b>FD1, FD2</b>		N/A	N/A					N/A	N/A	
<b>E, EL, EM</b>	N/A		N/A					N/A	N/A	
NOTE Refer to Clause 3 for abbreviated terms and definitions.										
<sup>a</sup> See 6.1 for general information on corresponding current impulse waveshapes.										
<sup>b</sup> See Figure 1 for arrester references in a typical modern LCC HVDC converter station. The actual arrangement is design specific.										
<sup>c</sup> STIPL for valve arresters only.										

## 7.3 Representative overvoltages ( $U_{rp}$ )

The representative overvoltage as defined in IEC 60071-11:–, 6.4, which are determined by considering relevant faults and examining the results of the calculation, can be presented as in Table 7.

**Table 7 – Representative overvoltages and required withstand voltages**

Insulation location (Refer to Figure 3)	Representative overvoltages ( $U_{rp}$ )			Required withstand voltages ( $U_{rw}$ )		
	SIPL RSFO	LIPL RFFO	STIPL <sup>a</sup> RSTO <sup>a</sup>	RSIWV	RLIWV	RSTIWV
	kV	kV	kV	kV	kV	kV
<b>I AC switchyard section</b>						
AC busbars and conventional equipment, 1-N			N/A			N/A
Filter capacitors (a) HV side, 1-N, 3-N (b) Across, 1-2, 3-N (c) LV side, 2-N			N/A			N/A
Filter reactors (a) HV side, 2-N, 3-N (b) Across, 2-3, 3-N (c) LV side, 3-N			N/A			N/A
<b>II Converter equipment</b>						
Across a valve, 5-9, 7-5, 6-7, 6-8						
Across lower valve group, 7-8			N/A			N/A
Across upper valve group, 9-7			N/A			N/A
Phase to phase within a six-pulse bridge, 5a-5b, 5b-5c, 5c-5a 6a-6b, 6b-6c, 6c-6a			N/A			N/A
Mid-point to earth, 7-G			N/A			N/A
Each converter unit HV side, 9-G			N/A			N/A
Each converter unit LV side, 8-G			N/A			N/A
Converter HVDC bus, 9-G			N/A			N/A
DC neutral bus, 8-G			N/A			N/A
<b>III DC side equipment</b>						
Across smoothing reactor, 10-9			N/A			N/A
Filter capacitors (a) HV side, 10-G, 12-G (b) Across, 10-11, 12-8 (c) LV side, 11-G, 8-G			N/A			N/A
Filter reactors (a) HV side, 11-G, 12-G (b) Across, 11-12, 12-8 (b) LV side, 12-G, 8-G			N/A			N/A
HVDC Line/Cable, 10-G			N/A			N/A
DC line, 10-G			N/A			N/A
Earth electrode line, 8-G			N/A			N/A

Insulation location (Refer to Figure 3)	Representative overvoltages ( $U_{rp}$ )			Required withstand voltages ( $U_{rw}$ )		
	SIPL RSFO	LIPL RFFO	STIPL <sup>a</sup> RSTO <sup>a</sup>	RSIWV	RLIWV	RSTIWV
	kV	kV	kV	kV	kV	kV
<b>IV Other equipment such as transformer, valve, windings (e.g., in oil)</b>						
Star winding (a) phase-to-neutral, 5a-n, 5b-n, 5c-n (b) phase to phase, 5a-5b, 5b-5c, 5c-5a (c) neutral to earth, n-G (d) phase-to-earth, 5a-G, 5b-G, 5c-G			N/A			N/A
Delta winding (a) phase to phase, 6a-6b, 6b-6c, 6c-6a (b) phase-to-earth, 6a-G, 6b-G, 6c-G			N/A			N/A
Star-winding to delta winding, 5-6			N/A			N/A
<sup>a</sup> STIPL, RSTO and RSTIWV are applicable to valve arresters only.						

#### 7.4 Determination of the co-ordination withstand voltages ( $U_{cw}$ )

The co-ordination withstand voltages ( $U_{cw}$ ) is calculated from the co-ordination factor ( $K_C$ ) and the representative overvoltages ( $U_{rp}$ ), or the deterministic co-ordination factor  $K_{cd}$  instead of  $K_C$  (for more details, refer to 6.5 of IEC 60071-11:–).

#### 7.5 Determination of the required withstand voltages ( $U_{rw}$ )

The required withstand voltages of equipment can be obtained by applying a factor to the corresponding protective level of the arrester (details refer to 6.6 of IEC 60071-11:–).

Table 3 in Clause 6 of IEC 60071-11:–, provides a set of indicative values for this factor.

#### 7.6 Determination of the specified withstand voltage ( $U_w$ )

The specified withstand voltages are values equal to or higher than the required withstand voltages. The determination principle refers to IEC 60071-11:–, 6.7.

## 8 Study tools and system modelling

### 8.1 General

Clause 8 discusses the overall methods and tools required to evaluate the overvoltage characteristics that can affect an HVDC converter station and to derive the required arrester characteristics. The objective of these studies, as further detailed in Clause 6, are as follows:

- determine stresses and protective levels of arresters in an HVDC converter station;
- form the basis for insulation co-ordination of HVDC converter stations;
- derive the specification of all the arresters involved.

### 8.2 Study approach and tools

In order to carry out the studies, the following information is required, as further detailed in 8.3:

- configuration of the HVDC station, as well as AC and DC system data;
- data of equipment connected on both the AC and DC side (e.g., transformers, lines, etc.);



- arrester characteristics appropriate to temporary overvoltage, slow-front, fast-front and steep-front impulses;
- converter control and valve protection strategies, including response and/or delay in valve protecting firing circuit;
- operating conditions;
- valve protective strategies (response of valve protective firing).

The overvoltage study approach can consist of the following steps:

Step 1: Define the preliminary arrester configuration and determine the preliminary arrester parameters such as  $U_c$ ,  $U_{ch}$ , PCOV and/or CCOV for each arrester.

Step 2: Study the cases producing the highest current and energy stresses. At this stage, the minimum number of arrester columns and their ratings are defined, considering the arrester stresses and contingencies.

Step 3: Check for fast-front and steep-front overvoltages to ensure that with the arrester arrangement defined in steps 1 and 2, the whole HVDC station is adequately protected. Additional arresters can be required due to distance effects.

Step 4: Establish the arrester duties (co-ordination current/voltage/energy) based on the study results and determine the arrester specification (see Clause 6).

Step 5: Establish the maximum overvoltages and withstand voltages at various locations (see 7.4).

For arrester duties, the general principles consist in considering the minimum V-I protection characteristics for energy consumption and the maximum V-I protection characteristics for the protection level.

Although there are many tools available for the calculation of overvoltages and arrester stresses, it is important to consider the validity of each tool, for the proper representation of power system components to obtain the required characteristics of the models for the study undertaken. To obtain meaningful results the components need to be properly modelled with regard to the frequency range of interest and other characteristics of the network components. (For guidance on model representations, see the Bibliography). Typically, digital computer programs employing numerical transient analysis methods are used for these calculations.

Study tools using real time digital simulation techniques are available. These tools under the present conditions cannot be suitable to study the high-frequency overvoltages due to time step limitations.

### **8.3 System details**

#### **8.3.1 Modelling and system representation**

For insulation co-ordination studies, models of network components valid in the range DC to 50 MHz can be required. A representation valid for the complete frequency range is difficult to achieve for all network components. Various parameters have different influences on the correct representation of components within the frequency range of interest at which the model should be representative of the system characteristics.

Transient phenomena appear during transitions from one steady state condition to another. The primary causes of such disturbances in a system are closing or opening of a breaker or another switching equipment, short-circuits, earth faults or lightning strikes. The consequential electromagnetic phenomena are travelling waves on lines, cables or busbar sections and oscillations between inductances and capacitances of the system. The frequencies of oscillations are determined by the surge impedances and travel times of the connecting lines.

Table 8 gives an overview on the various origins of such transients and their frequency ranges. These frequency ranges are needed for modelling.

**Table 8 – Origin of overvoltages and associated frequency ranges**

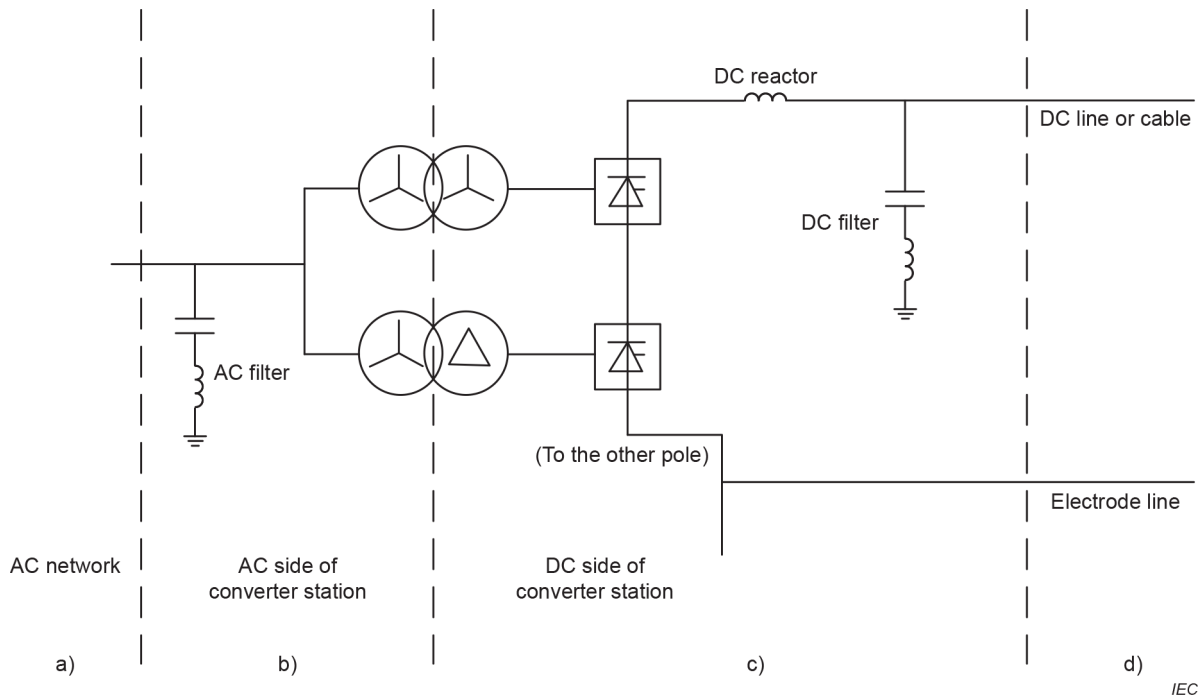
Group	Frequency range for representation	Representation mainly for	Origin
I	0,1 Hz to 3 kHz	Temporary overvoltages	Transformer energization (ferroresonance) Load rejection Fault clearing or initiation, line energization
II	50 Hz to 20 kHz	Slow-front overvoltages	Terminal faults Short line faults Closing/reclosing
III	10 kHz to 3 MHz	Fast-front overvoltages	Circuit breaker restrikes Faults in substations
IV	1 MHz to 50 MHz	Steep-front overvoltages	Disconnecter switching Faults in GIS – substations Flashover

The overall system configuration is schematically represented in Figure 8. From an insulation co-ordination point of view, it is convenient to divide an HVDC converter station, include the connected AC and DC lines, into different parts with regard to the overvoltages generated.

These parts or subsystems comprise:

- a) the AC network;
- b) the AC part of the HVDC converter station including the AC filters and any other reactive power source, circuit breakers and line side of converter transformer;
- c) the converter bridges, the valve side of the converter transformer. The dc reactor, the DC filter and the neutral bus;
- d) the DC line/cable and earth electrode line/cable.

These parts or subsystems should be considered in defining the study model. which could be either detailed or suitably simplified without losing the validity of the study results.



**Figure 8 – One pole of an LCC HVDC converter station**

### 8.3.2 AC network and AC side of the LCC HVDC converter station

#### 8.3.2.1 Temporary and slow-front overvoltages

Details about the AC network and AC side equipment, and the modelling adequate for slow-front and temporary overvoltages are dealt with in 8.3.2.1.

- Detailed three-phase modelling or adequate equivalents for the AC network near the HVDC converter station. Lines leaving the station and nearby transformers including their saturation characteristics are represented as well as converters electrically close to the plant. Network equivalents should be used for the main part of the AC systems, and the damping effect of the loads which affect the overall damping at resonance frequencies as seen from the HVDC station is taken into account.
- Representation of the equipment installed on the AC side of the HVDC converter station. This includes any reactive power source and the converter transformers. The saturation of the converter transformer is a key parameter.
- Representation of AC bus and filter arrester characteristics in the frequency range of some hundreds of Hz.

#### 8.3.2.2 Fast-front and steep-front overvoltages

Details about the AC network and AC side equipment, and the modelling adequate for fast-front and steep-front overvoltages are dealt with in this 8.3.2.2.

An adequate high frequency parameter model should be used for AC lines, busbars, etc.

- AC filter components shall be represented including stray inductance and capacitance.
- AC lines of length such that the travelling time exceeds the time frame of the studied event can be represented by their surge impedance.
- All stray capacitances of equipment made up of windings can be represented by lumped equivalents, both to earth and across the equipment.
- Arrester characteristics shall be considered for the appropriate frequency range as given in Table 7.

- e) There shall be an adequate model for the earthing system, the earth connection and the flashover arc.

### **8.3.3 DC overhead line/cable and earth electrode line details**

#### **8.3.3.1 Temporary and slow-front overvoltages**

Details about the DC overhead line/cable and electrode line, and the modelling adequate for slow-front and temporary overvoltages are dealt with in 8.3.3.1.

- a) DC lines and earth electrode lines shall be represented from DC up to about the 20 kHz frequency range according to Table 7.
- b) Representation of DC and neutral bus arresters characteristics in the frequency range of some hundreds of Hz.

#### **8.3.3.2 Fast-front and steep-front overvoltages**

Details about the DC overhead line/cable and electrode line, and the modelling adequate for fast-front and steep-front overvoltages are dealt with in 8.3.3.2.

- a) Adequate high-frequency parameters should be used for DC and earth electrode lines as well as buses. Also, short lines can be represented by their surge impedances as long as the reflection from their far end does not intercept with the studied event. The 50 % flashover voltages of the line insulators are decisive for the maximum stresses.
- b) DC arresters and neutral bus arresters characteristics should be considered for the appropriate frequency range as given in Table 3 from IEC 60071-11:–.
- c) There shall be an adequate model for the earth connection and flashover arc.

### **8.3.4 DC side of an LCC HVDC converter station details**

#### **8.3.4.1 Temporary and slow-front overvoltages**

Details about the converter station equipment on the DC side, and the modelling adequate for slow-front and temporary overvoltages are dealt with in 8.3.4.1.

- a) DC side station equipment (DC reactor, valves, DC filter and neutral bus arresters and capacitor, etc.) is represented.
- b) Representation of DC side arresters in the frequency range of some hundreds of Hz.
- c) If applicable, control and protection actions shall be considered, particularly for temporary overvoltages.

#### **8.3.4.2 Fast-front and steep-front overvoltages**

Details about the converter station equipment on the DC side, and the modelling adequate for fast-front and steep-front overvoltages are dealt with in this 8.3.4.2.

- a) DC side equipment (DC reactor, DC filters, valves etc.) shall be represented including stray inductances and capacitances.
- b) All stray capacitances of equipment made up of windings can be represented by lumped equivalents, both to earth and across equipment.
- c) Arrester characteristics for the appropriate frequency range shall be indicated.
- d) Control and protection actions do not need to be considered since they will not respond to these fast transients.

## Annex A (informative)

### Example of insulation co-ordination for LCC HVDC converter stations

#### A.1 General

Annex A gives a description and method of calculation for the insulation co-ordination of a LCC HVDC converter station with a DC line or cable with earth return. Two examples are presented. One is for LCC HVDC converter station in a pole with one 12-pulse converter (see Clause A.2), the other is for LCC HVDC converter station in a pole with two 12-pulse converters in series (see Clause A.3). These examples are intended to be informative and tutorial and is very schematic. It mainly summarizes steps leading to chosen arrester ratings and specified insulation levels, based on procedures explained in the main text.

The results presented in Annex A are based on the study approach and the described procedures in Clause 8 and in Clause 6. For the specified withstand voltages of HVDC equipment, calculated values for SIWV, LIWV and SSFIWV are rounded up to convenient practical values. It is proposed that the value could be selected as close as possible to the value given in Annex C of IEC 60071-11:–.

#### A.2 Example for LCC HVDC converter station in a pole with one 12-pulse converter

##### A.2.1 Arrester protective scheme

Figure A.1 shows the arrester protective schemes for LCC HVDC converter station in a pole with one 12-pulse converter. All arresters are of the metal-oxide type without gap.

##### A.2.2 Arrester stresses, protection and insulation levels

###### A.2.2.1 General

The following main data are used for the basic design of LCC HVDC converter station with one 12-pulse converter:

AC side: strong AC system

DC side:	Unit		
DC voltage	kV	500	(rectifier)
DC current	A	1 500	
Smoothing reactor	mH	225	
Firing angles	degree (°)	15/17	(rectifier/inverter)

Converter transformer:	Unit	
Rating (three-phase, six-pulse)	MVA	459
Short-circuit impedance	p.u.	0,12
Valve side voltage	kV r.m.s.	204
Tap-changer range		±5 %
Inductance per phase (valve side)	mH	35

AC bus arrester (A):

The following data are given for the LCC HVDC converters:

Parameters		Bus 1 (A)
Nominal system voltage	kV r.m.s	400
Highest system voltage ( $U_s$ )	kV r.m.s	420
Continuous operating voltage, phase-to-earth	kV r.m.s	243
SIPL (at 1,5 kA)	kV	632
LIPL (at 10 kA)	kV	713
Maximum slow-front overvoltage transferred to valve side (between two phases)	kV	549
Number of parallel arrester columns	–	2
Arrester energy capability	MJ	3,2

Valve arrester type (V1) and (V2):

The following values are valid for both converter stations:

CCOV	kV	$208 \times \sqrt{2}$	
Number of parallel columns		8	for arrester (V1)
		2	for arrester (V2)
Energy capability	MJ	16,2	for arrester (V1)
	MJ	2,6	for arrester (V2)

The stresses of the valve arresters are determined by computer studies for the following cases:

#### A.2.2.2 Slow-front overvoltages transferred from the AC side

The highest stresses are expected if the transferred slow-front overvoltage appears between two phases (e.g., R and S), where only one valve is conducting (Figure A.2). The value of the transferred slow-front overvoltage is dependent on the maximum protective level of the AC bus arrester (A) on the line side of the converter transformer.

Figure A.3 show the results for the LCC HVDC converters if only one arrester in the circuit is conducting. This fault case is decisive for the design of all lower valve arresters type (V2).

Results (valid for valve arrester (V2)):

The switching impulse protective level (SIPL) of the valve arrester (V2) is given by

$$\begin{aligned} \text{SIPL} &= 500 \text{ kV} && \text{at } 1\,027 \text{ A (see Figure A.3)} \\ \text{RSIWV} &= 1,15 \times 500 \text{ kV} &= 575 \text{ kV} &\Rightarrow \boxed{\text{SIWV} = 575 \text{ kV}} \end{aligned}$$

#### A.2.2.3 Earth fault between valve and upper bridge transformer bushing

This fault case gives the highest stresses for the valve arresters protecting the three-pulse commutating group on the highest potential. The equivalent circuit for this case is shown in Figure A.4. The stresses for the upper valve arresters are also dependent on the fault insertion time. To determine the maximum values, the time of fault access shall be changed by several electrical angle between 0 to 360 degrees.

The results of the maximum stresses are shown in Figure A.5.

This fault case is decisive for the design of all upper valve arresters (V1) if the slow-front overvoltage (A.2.2.2) does not result in higher arrester stresses.

Results (valid for valve arrester (V1)):

The switching impulse protective level (SIPL) of the valve arrester (V1) is given by

$$\begin{aligned} \text{SIPL} &= 499,8 \text{ kV} && \text{at } 4\,230 \text{ A (see Figure A.5)} \\ \text{RSIWV} &= 1,15 \times 499,8 \text{ kV} &= 575 \text{ kV} &\Rightarrow \boxed{\text{SIWV} = 575 \text{ kV}} \end{aligned}$$

Converter group arrester (C)

The following values are valid for both converter stations:

CCOV:	558 kV
Number of parallel columns:	1
Energy capability:	2,5 MJ

The stresses of the group arresters are defined by transferred slow-front overvoltages from the AC side and should be determined by computer studies. The magnitude of the transferred slow-front overvoltage is twice the value given for the valve arresters. It is assumed that during normal operation, when four thyristor valves are conducting, a slow-front overvoltage will be transferred between the phases.

For the design of the converter group arrester (C) the following values for the co-ordination currents are chosen:

$$\begin{aligned} \text{SIPL} &= 930 \text{ kV} && \text{at } 0,5 \text{ kA} \\ \text{LIPL} &= 1\,048 \text{ kV} && \text{at } 2,5 \text{ kA} \\ \text{RSIWV} &= 1,15 \times 930 \text{ kV} &= 1\,070 \text{ kV} &\Rightarrow \boxed{\text{SIWV} = 1\,175 \text{ kV}} \\ \text{RLIWV} &= 1,20 \times 1\,048 \text{ kV} &= 1\,258 \text{ kV} &\Rightarrow \boxed{\text{LIWV} = 1\,300 \text{ kV}} \end{aligned}$$

DC bus arrester (DB)

The following values are valid for both converter stations:

CCOV:	515 kV
Number of parallel columns:	1
Energy capability:	2,2 MJ

For the design of the DC bus arrester (DB) the following values for the co-ordination currents are chosen:

$$\begin{aligned} \text{SIPL} &= 866 \text{ kV} && \text{at } 1 \text{ kA} \\ \text{LIPL} &= 977 \text{ kV} && \text{at } 5 \text{ kA} \\ \text{RSIWV} &= 1,15 \times 866 \text{ kV} &= 996 \text{ kV} &\Rightarrow \boxed{\text{SIWV} = 1\,050 \text{ kV}} \\ \text{RLIWV} &= 1,2 \times 977 \text{ kV} &= 1\,173 \text{ kV} &\Rightarrow \boxed{\text{LIWV} = 1\,300 \text{ kV}} \end{aligned}$$

DC line/cable arrester (DL)

## IS/IEC 60071-12 : 2022

The following values are valid for both ends of the DC line/cable arrester (DL):

CCOV:	515 kV
Number of parallel columns:	8
Energy capability:	17,0 MJ

For the design of the DC line/cable arresters (DL) the following values for the co-ordination currents are chosen:

SIPL	=	807 kV		at 1 kA		
LIPL	=	872 kV		at 5 kA		
RSIWV	=	$1,15 \times 807$ kV	=	928 kV	⇒	<u>SIWV = 950 kV</u>
RLIWV	=	$1,20 \times 872$ kV	=	1 046 kV	⇒	<u>LIWV = 1 050 kV</u>

### Neutral bus arrester (E)

The following values are valid for both converter stations comprising all neutral bus arresters:

CCOV:	30 kV
Number of parallel columns:	12
Energy capability:	2,4 MJ

For the design of all neutral bus arresters (E) the following values for the co-ordination currents are chosen:

SIPL	=	78 kV		at 2 kA		
LIPL	=	88 kV		at 10 kA		
RSIWV	=	$1,15 \times 78$ kV	=	90 kV	⇒	<u>SIWV = 125 kV</u>
RLIWV	=	$1,20 \times 88$ kV	=	106 kV	⇒	<u>LIWV = 125 kV</u>

### AC filter arrester (FA)

The operating voltage for the arresters consists of fundamental and harmonic voltages.

The rating of the arresters is determined by the stresses during earth faults followed by recovery overvoltages on the AC bus.

### AC filter arrester (FA1)

$U_{ch}$ :	60 kV
Number of parallel columns:	2
Energy capability:	1,0 MJ

For the design of the arrester (FA1) the following values for the co-ordination currents are chosen:

SIPL	=	158 kV		at 2 kA		
LIPL	=	192 kV		at 40 kA		
RSIWV	=	$1,15 \times 158$ kV	=	182 kV	⇒	<u>SIWV = 200 kV</u>
RLIWV	=	$1,20 \times 192$ kV	=	230 kV	⇒	<u>LIWV = 250 kV</u>



## AC filter arrester (FA2)

$U_{ch}$ :	30 kV
Number of parallel columns:	2
Energy capability:	0,5 MJ

For the design of the arrester (FA2) the following values for the co-ordination currents are chosen:

SIPL	=	104 kV		at 2 kA		
LIPL	=	120 kV		at 10 kA		
RSIWV	=	$1,15 \times 104$ kV	=	120 kV	⇒	<span style="border: 1px solid black; padding: 2px;">SIWV = 150 kV</span>
RLIWV	=	$1,20 \times 120$ kV	=	144 kV	⇒	<span style="border: 1px solid black; padding: 2px;">LIWV = 150 kV</span>

## DC filter arrester (FD)

The operating voltage for the arresters consists mainly of harmonic voltages.

The rating of the arresters is determined by the stresses during transferred slow-front overvoltage with a subsequent earth fault on the DC bus.

## DC filter arrester (FD1)

$U_{ch}$ :	5 kV
Number of parallel columns:	2
Energy capability:	0,8 MJ

For the design of the arrester (FD1) the following values for the co-ordination currents are chosen:

SIPL	=	136 kV		at 2 kA		
LIPL	=	184 kV		at 40 kA		
RSIWV	=	$1,15 \times 136$ kV	=	156 kV	⇒	<span style="border: 1px solid black; padding: 2px;">SIWV = 200 kV</span>
RLIWV	=	$1,20 \times 184$ kV	=	221 kV	⇒	<span style="border: 1px solid black; padding: 2px;">LIWV = 250 kV</span>

## DC filter arrester (FD2)

$U_{ch}$ :	5 kV
Number of parallel columns:	2
Energy capability:	0,5 MJ

For the design of the arrester (FD2) the following values for the co-ordination currents are chosen:

SIPL	=	104 kV		at 2 kA		
LIPL	=	120 kV		at 10 kA		
RSIWV	=	$1,15 \times 104$ kV	=	120 kV	⇒	<span style="border: 1px solid black; padding: 2px;">SIWV = 150 kV</span>
RLIWV	=	$1,20 \times 120$ kV	=	144 kV	⇒	<span style="border: 1px solid black; padding: 2px;">LIWV = 150 kV</span>

### A.2.3 Transformer valve side withstand voltages

#### A.2.3.1 Phase-to-phase

Since the converter transformer valve windings are not directly protected by a single arrester, the following two cases are considered:

when the valves are conducting, the phase-to-phase insulation of the converter transformer valve side is protected by one valve arrester (V);

when the valves are blocked, two valve arresters (V) are connected in series, phase-to-phase. During this event, the full transferred slow-front overvoltage will determine the maximum slow-front overvoltage.

$$\text{SIPL} = 550 \text{ kV}$$

$$\text{RSIWL} = 1,15 \times \text{SIPL}$$

The selected specified lightning withstand voltage is:

$$\boxed{\text{SIWV} = 650 \text{ kV}}$$

$$\boxed{\text{LIWV} = 750 \text{ kV}}$$

If the two phases are in separate transformer units (single-phase, three-winding transformers), and under the assumption that the voltages are not equally shared, the specified insulation levels for the star-winding have been selected to be:

$$\boxed{\text{SIWV} = 550 \text{ kV}}$$

$$\boxed{\text{LIWV} = 650 \text{ kV}}$$

#### A.2.3.2 Upper bridge transformer phase-to-earth (star)

The phase-to-earth insulation of the transformer and converters is determined by additive slow-front overvoltages between the transformer phases during the conducting status. These slow-front overvoltages originating from the AC side are limited by the arrester (A) on the primary side of the converter transformer. This additive method is not possible in the non-conducting status of the thyristor valves. Therefore, only the 'conducting' status needs to be considered.

$$\text{SIPL} = 1\,000 \text{ kV} \quad (2 \times \text{SIPL of arrester (V2) at } 1\,025 \text{ A, assuming no current in the neutral arrester})$$

$$\text{RSIWV} = 1,15 \times \text{SIPL} \quad \Rightarrow \quad \boxed{\text{SIWV} = 1\,175 \text{ kV}}$$

The selected specified lightning withstand voltage is:  $\boxed{\text{LIWV} = 1\,300 \text{ kV}}$

#### A.2.3.3 Lower bridge transformer phase-to-earth (delta)

The insulation levels are the same as phase-to-phase, assuming no current in the neutral arrester.

$$\boxed{\text{SIWV} = 650 \text{ kV}}$$

The selected specified lightning withstand voltage is:

$$\boxed{\text{LIWV} = 750 \text{ kV}}$$

### A.2.4 Air-insulated smoothing reactors withstand voltages

#### A.2.4.1 Terminal-to-terminal slow-front overvoltages

The worst case for the stresses between the terminals of smoothing reactors is given by the slow-front overvoltages on the DC side, which is limited by the arrester (DL). Assuming opposite polarity to the DC voltage, the total voltage will be:

SIPL of arrester (DL):	866 kV
Maximum DC voltage:	500 kV
Sum of both voltages:	1 366 kV
Smoothing reactors:	225 mH
Transformer inductances:	140 mH (4 × 35 mH)
Total inductance:	365 mH
Voltage between terminals:	$1\,366\text{ kV} \times (225\text{ mH}/365\text{ mH}) = 842\text{ kV}$

$$\text{SIPL} = 842\text{ kV}$$

$$\text{RSIWV} = 1,15 \times 842\text{ kV} = 968\text{ kV} \Rightarrow \boxed{\text{SIWV} = 1\,175\text{ kV}}$$

The maximum fast-front overvoltages between terminals are determined by the relative ratio of the capacitance across the reactor to the capacitance to earth on the valve side of the reactor. The specified lightning withstand voltage is:

$$\boxed{\text{LIWV} = 1\,300\text{ kV}}$$

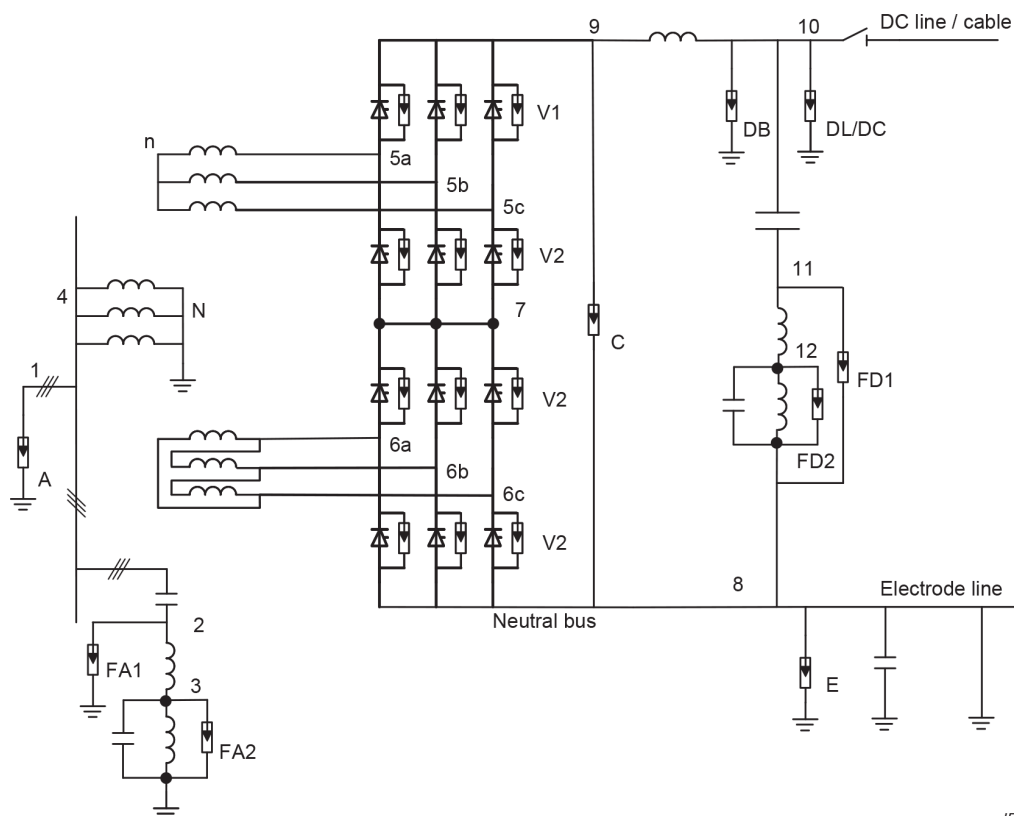
#### A.2.4.2 Terminal-to-earth

The insulation levels are the same as for the arresters (C) or (DL).

$$\boxed{\text{SIWV} = 1\,175\text{ kV}}$$

$$\boxed{\text{LIWV} = 1\,300\text{ kV}}$$

A.2.5 Results



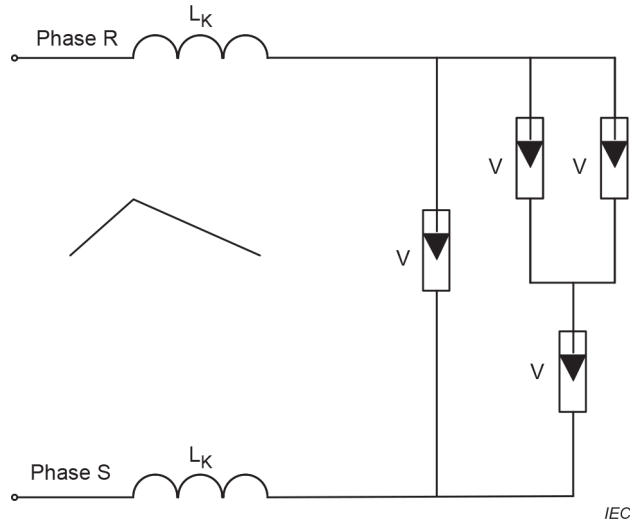
Arrester type		A	V1	V2	C	DB	DL	E	FD1	FD2	FA1	FA2
$U_{ch}$ or CCOV	kV	243 r.m.s.	294 crest	294 crest	558 crest	515 DC	515 DC	30 DC	5 DC	5 DC	60 r.m.s.	30 r.m.s.
Lightning:												
– protection level	kV	713	–	–	1 048	977	872	88	184	120	192	120
– at current	kA	10	–	–	2,5	5	5	10	40	10	40	10
Switching:												
– protection level	kV	632	499,8	500	930	866	807	78	136	104	158	104
– at current	kA	1,5	4,23	1,025	0,5	1,0	1,0	6,0	2,0	2,0	2,0	2,0
No. of columns	–	2	8	2	1	1	8	2	2	2	2	2
Energy capability	MJ	9,2	10,4	2,6	2,5	2,2	17,0	0,4	0,8	0,5	1,0	0,5

Protection location	1	2	3	4	5	6	7	8	9	10	11	12
$U_{ch}$ (kV)	243	60	30	243	558	294	294	30	558	515	15	15
LIPL = RFFO (kV)	713	192	120	713	–	–	–	88	1 048	977	184	120
SIPL = RSFO (kV)	632	158	104	632	1 000	550	550	78	930	866	136	104
LIWV (kV)	1 425	250	150	1 425	1 300	750	750	125	1 300	1 300	250	150
SIWV (kV)	1 050	200	150	1 050	1 175	650	650	125	1 175	1 175	200	150

Protection location	1-2	2-3		5 and 6 ph-ph	5-6	8-9	9-10	10-11	11-12	Valves V1 and V2
LIPL = RFFO (kV)	825	192		–	–	1048	–	977	184	–
SIPL = RSFO (kV)	747	158		550	1 000	930	842	866	136	500
LIWV (kV)	1 300	250		750	1 300	1 300	1 300	1 300	250	–
SIWV (kV)	1 050	200		650	1 175	1 175	1 175	1 175	200	575

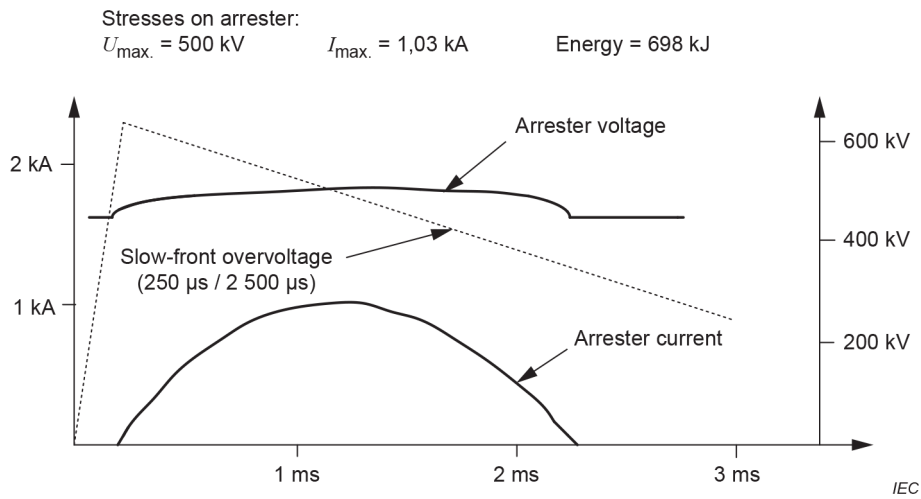
NOTE Specified withstand voltages on the AC side are in line with recommended standard withstand values in IEC 60071-1 for 420 kV AC standard voltage class.

Figure A.1 – AC and DC arresters (LCC HVDC converter station in a pole with one 12-pulse converter)

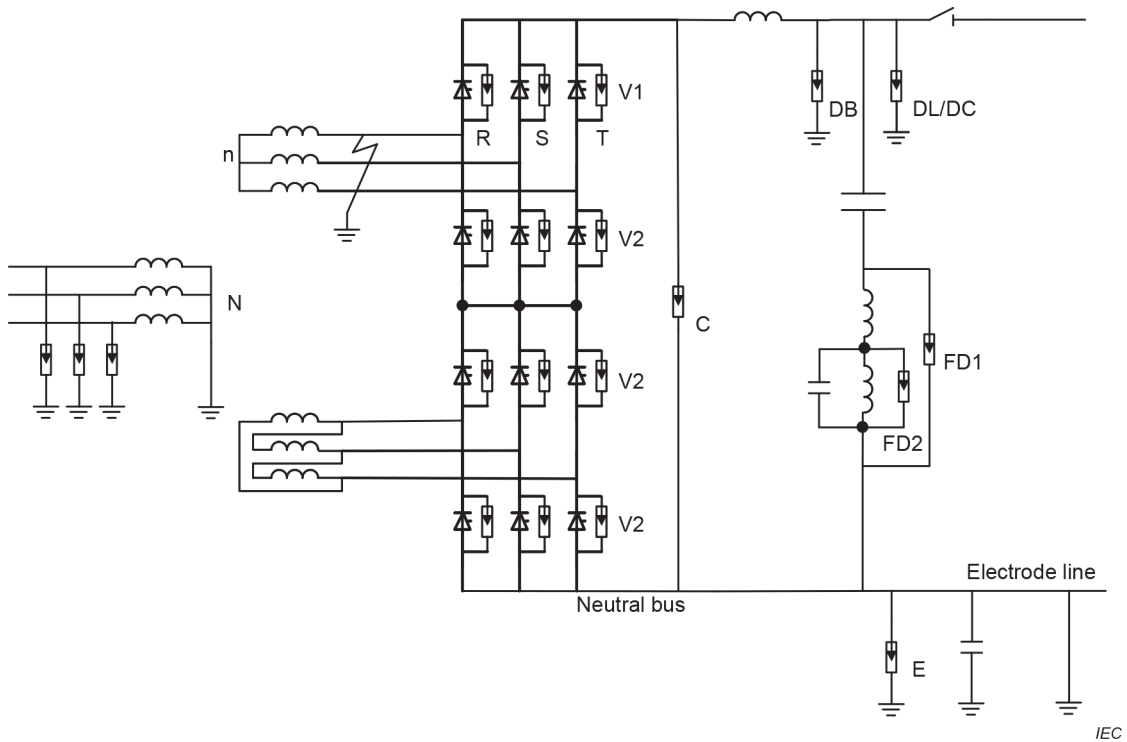


NOTE The stray capacitances are not shown, but they are design dependent.

**Figure A.2 – Valve arrester stresses for slow-front overvoltages from AC side**

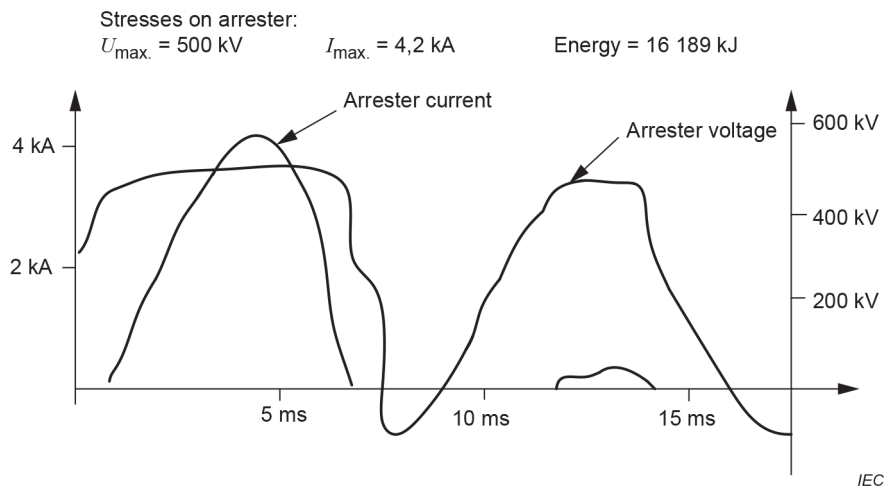


**Figure A.3 – Arrester V2 stress for slow-front overvoltage from AC side**



NOTE The stray capacitances are not shown and are design dependent.

**Figure A.4 – Valve arrester stresses for earth fault between valve and upper bridge transformer bushing**



**Figure A.5 – Arrester V1 stress for earth fault between valve and upper bridge transformer bushing**

**A.3 Example for LCC HVDC converter station in a pole with two 12-pulse converters in series**

**A.3.1 Arrester protective scheme**

Figure A.6 shows the arrester protective schemes for LCC HVDC converter station in a pole with two 12-pulse converters in series. All arresters are of the metal-oxide type without gap.

### A.3.2 Arrester stresses, protection and insulation levels

#### A.3.2.1 General

The following main data are used for the basic design of the LCC HVDC converter station in a pole with two 12-pulse converters in series.

AC side: strong AC system

DC side:	Unit		
DC voltage	kV	800	
DC current	A	3 125	
Pole line smoothing reactor	mH	150	
Neutral bus smoothing reactor	mH	150	
Firing angles	degree (°)	15/18,67	(rectifier/inverter)

Converter transformer:	Unit	
Rating (single-phase)	MVA	250,21
Short-circuit impedance	p.u.	0,18
Valve side voltage (star)	kV	169,85
Tap-changer range		±1,25 %
Inductance per phase (valve side)	mH	22

AC bus arrester (A):

The following data are given for the LCC HVDC converters:

Parameters		Bus A
Nominal system voltage	kV (r.m.s)	500
Highest system voltage ( $U_s$ )	kV (r.m.s)	550
Continuous operating voltage, phase-to-earth	kV (r.m.s)	318
SIPL (at 2 kA)	kV	780
LIPL (at 20 kA)	kV	907
Arrester energy capability	MJ	8,9

Valve arrester type (V1), (V2) and (V3):

The following values are valid for both converter stations:

CCOV	kV	245	
Number of parallel columns		8	for arrester (V1)
		4	for arrester (V2)
		2	for arrester (V3)
Energy capability	MJ	10	for arrester (V1)
	MJ	5	for arrester (V2)
	MJ	2,6	for arrester (V3)

The stresses of the valve arresters are determined by computer studies for the following cases:

### A.3.2.2 Slow-front overvoltages transferred from the AC side

The highest stresses are expected if the transferred slow-front overvoltage appears between two phases, where only one valve is conducting (Figure A.2). The value of the transferred slow-front overvoltage is dependent on the maximum protective level of the AC bus arrester (A) on the line side of the converter transformer.

When the slow-front overvoltage at the AC side is transmitted through the converter transformer, it has the greatest effect on the arrester V3. This fault case is decisive for the design of arresters (V3).

Results (valid for valve arrester (V3)):

The switching impulse protective level (SIPL) of the valve arrester (V3) is given by

$$\begin{array}{llllll}
 \text{SIPL} & = & 395 \text{ kV} & \text{at } 1 \text{ kA} & & \\
 \text{LIPL} & = & 395 \text{ kV} & \text{at } 0,6 \text{ kA} & & \\
 \text{RSI WV} & = & 1,15 \times 395 \text{ kV} & = & 454 \text{ kV} & \Rightarrow \boxed{\text{SI WV} = 454 \text{ kV}} \\
 \text{RLI WV} & = & 1,15 \times 395 \text{ kV} & = & 454 \text{ kV} & \Rightarrow \boxed{\text{LI WV} = 454 \text{ kV}}
 \end{array}$$

### A.3.2.3 Upper bridge transformer bushing to earth fault while lower 400 kV converter unit operating alone

This fault exerts the maximum stress on the valve arrester of three pulse converter group with the highest potential of lower 400 kV converter unit. The effect on high potential valve arrester also depends on the starting time of fault. In order to determine the maximum effect, the time of fault access shall be changed by electrical angle from 0 to 360.

This fault case is decisive for the design of upper bridge arresters (V2) of lower 400 kV converter unit.

Results (valid for valve arrester (V2)):

The switching impulse protective level (SIPL) of the valve arrester (V2) is given by

$$\begin{array}{llllll}
 \text{SIPL} & = & 395 \text{ kV} & \text{at } 2 \text{ kA} & & \\
 \text{LIPL} & = & 395 \text{ kV} & \text{at } 1,2 \text{ kA} & & \\
 \text{RSI WV} & = & 1,15 \times 395 \text{ kV} & = & 454 \text{ kV} & \Rightarrow \boxed{\text{SI WV} = 454 \text{ kV}} \\
 \text{RLI WV} & = & 1,15 \times 395 \text{ kV} & = & 454 \text{ kV} & \Rightarrow \boxed{\text{LI WV} = 454 \text{ kV}}
 \end{array}$$

### A.3.2.4 Earth fault between valve and upper bridge transformer bushing

This fault exerts the maximum stress on the valve arrester of three pulse converter group with the highest potential of higher 400 kV converter unit. The effect on high potential valve arrester also depends on the starting time of fault. In order to determine the maximum effect, the time of fault access shall be changed by electrical angle from 0 to 360.

This fault case is decisive for the design of upper bridge arresters (V1) of higher 400 kV converter unit.

Results (valid for valve arrester (V1)):

The switching impulse protective level (SIPL) of the valve arrester (V1) is given by



SIPL	=	395 kV		at 4 kA		
LIPL	=	395 kV		at 2,4 kA		
RSIWV	=	$1,15 \times 395 \text{ kV}$	=	454 kV	⇒	<u>SIWV = 454 kV</u>
RLIWV	=	$1,15 \times 395 \text{ kV}$	=	454 kV	⇒	<u>LIWV = 454 kV</u>

#### DC bus arrester (DB)

The following values are valid for both converter stations:

CCOV:	816 kV
Number of parallel columns:	2
Energy capability:	9 MJ

For the design of the DC bus arrester (DB) the following values for co-ordination currents are chosen:

SIPL	=	1 328 kV		at 1 kA		
LIPL	=	1 579 kV		at 10 kA		
RSIWV	=	$1,15 \times 1 328 \text{ kV}$	=	1 527 kV	⇒	<u>SIWV = 1 600 kV</u>
RLIWV	=	$1,20 \times 1 579 \text{ kV}$	=	1 894 kV	⇒	<u>LIWV = 1 950 kV</u>

#### DC line arrester (DL)

The following values are valid for DC line arrester:

CCOV:	816 kV
Number of parallel columns:	2
Energy capability:	9 MJ

DC line arrester (DL) consists of two D-type arresters. For the design of the DC line arrester (DL) the following values for co-ordination currents are chosen:

SIPL	=	1 328 kV		at 2 kA		
LIPL	=	1 579 kV		at 20 kA		
RSIWV	=	$1,15 \times 1 328 \text{ kV}$	=	1 527 kV	⇒	<u>SIWV = 1 600 kV</u>
RLIWV	=	$1,20 \times 1 579 \text{ kV}$	=	1 894 kV	⇒	<u>LIWV = 1 950 kV</u>

#### HV converter unit arrester (CH)

The following values are valid for HV converter unit arrester:

CCOV:	477 kV
Number of parallel columns:	2
Energy capability:	4,6 MJ

The stresses of the HV converter unit arrester are defined by the loss of AC power supply at the inverter side when the HV converter unit operates alone (LV converter unit is out of service) and should be determined by computer studies.

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For the design of the HV converter unit arrester (CH) the following values for co-ordination currents are chosen:

SIPL	=	706 kV	at 1 kA		
LIPL	=	791 kV	at 5 kA		
RSIWV	=	$1,15 \times 706$ kV	=	812 kV	$\Rightarrow$ <span style="border: 1px solid black; padding: 2px;">SIWV = 950 kV</span>
RLIWV	=	$1,20 \times 791$ kV	=	949 kV	$\Rightarrow$ <span style="border: 1px solid black; padding: 2px;">LIWV = 1 175 kV</span>

### Arrester between converters unit (CM)

The following values are valid for the arrester between converters unit:

CCOV:	477 kV
Number of parallel columns:	2
Energy capability:	4,6 MJ

For the design of the arrester between converters unit (CM) the following values for co-ordination currents are chosen:

SIPL	=	706 kV	at 1 kA		
LIPL	=	791 kV	at 5 kA		
RSIWV	=	$1,15 \times 706$ kV	=	812 kV	$\Rightarrow$ <span style="border: 1px solid black; padding: 2px;">SIWV = 950 kV</span>
RLIWV	=	$1,20 \times 791$ kV	=	949 kV	$\Rightarrow$ <span style="border: 1px solid black; padding: 2px;">LIWV = 1 175 kV</span>

### Mid-point bridge arrester (LV bridge) (ML)

The following values are valid for mid-point bridge arrester (LV bridge):

CCOV:	245 kV
Number of parallel columns:	2
Energy capability:	2,8 MJ

For the design of the Mid-point bridge arrester (LV bridge) (ML) the following values for co-ordination currents are chosen:

SIPL	=	435 kV	at 1 kA		
LIPL	=	447 kV	at 1 kA		
RSIWV	=	$1,15 \times 435$ kV	=	500 kV	$\Rightarrow$ <span style="border: 1px solid black; padding: 2px;">SIWV = 550 kV</span>
RLIWV	=	$1,20 \times 447$ kV	=	536 kV	$\Rightarrow$ <span style="border: 1px solid black; padding: 2px;">LIWV = 750 kV</span>

### DC neutral bus arrester (E)

The following values are valid for DC neutral bus arrester:

CCOV:	< 120 kV
Number of parallel columns:	4
Energy capability:	3,6 MJ

For the design of the DC neutral bus arrester (E) the following values for co-ordination currents are chosen:

SIPL	=	263 kV		at 1 kA		
LIPL	=	320 kV		at 20 kA		
RSIWV	=	$1,15 \times 263$ kV	=	302 kV	⇒	<span style="border: 1px solid black; padding: 2px;">SIWV = 325 kV</span>
RLIWV	=	$1,20 \times 320$ kV	=	384 kV	⇒	<span style="border: 1px solid black; padding: 2px;">LIWV = 450 kV</span>

Transformer valve winding arrester (T)

The following values are valid for transformer valve winding arrester:

CCOV:		885 kV
Number of parallel columns:		2
Energy capability:		9 MJ

For the design of the transformer valve winding arrester (T) the following values for co-ordination currents are chosen:

SIPL	=	1 344 kV		at 1 kA		
LIPL	=	1 344 kV		at 0,6 kA		
RSIWV	=	$1,15 \times 1 344$ kV	=	1 546 kV	⇒	<span style="border: 1px solid black; padding: 2px;">SIWV = 1 600 kV</span>
RLIWV	=	$1,20 \times 1 344$ kV	=	1 613 kV	⇒	<span style="border: 1px solid black; padding: 2px;">LIWV = 1 800 kV</span>

Smoothing reactor arrester (DR)

The following values are valid for smoothing reactor arrester:

CCOV:		40 kV
Number of parallel columns:		1
Energy capability:		2 MJ

For the design of the smoothing reactor arrester (DR) the following values for co-ordination currents are chosen:

SIPL	=	641 kV		at 3 kA		
LIPL	=	719 kV		at 10 kA		
RSIWV	=	$1,15 \times 641$ kV	=	737 kV	⇒	<span style="border: 1px solid black; padding: 2px;">SIWV = 750 kV</span>
RLIWV	=	$1,20 \times 719$ kV	=	863 kV	⇒	<span style="border: 1px solid black; padding: 2px;">LIWV = 950 kV</span>

### A.3.3 Transformer valve side withstand voltages

#### A.3.3.1 Phase-to-phase

The phase-to-phase protection of the valve side of converter transformer will be assumed by A' type arrester, whose protection level is calculated to be equal to the SIPL of A type arrester after being transferred to the valve side at the transformation ratio of the minimum tap changer. The SIPL of A type arrester is 780 kV and 273 kV after being transferred to the valve side. The phase-to-phase protection level is 473 kV.

RLIWV	=	$1,15 \times 473$ kV	=	543 kV	⇒	<span style="border: 1px solid black; padding: 2px;">SIWV = 650 kV</span>
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RLIWV is selected as 654 kV based on the ratio of switching impulse withstand voltage to lightning impulse withstand voltage of 0,83.

$$\text{RLIWV} = 654 \text{ kV} = \Rightarrow \boxed{\text{LIWV} = 750 \text{ kV}}$$

#### A.3.3.2 HV bridge transformer phase-to-earth (star)

Impulse protection level of arrester (T) is selected as:

$$\begin{aligned} \text{SIPL} &= 1\,344 \text{ kV} && \text{at } 1 \text{ kA} \\ \text{LIPL} &= 1\,344 \text{ kV} && \text{at } 0,6 \text{ kA} \\ \text{RSIWV} &= 1,15 \times 1\,344 \text{ kV} = 1\,546 \text{ kV} && \Rightarrow \boxed{\text{SIWV} = 1\,600 \text{ kV}} \\ \text{RLIWV} &= 1,20 \times 1\,344 \text{ kV} = 1\,613 \text{ kV} && \Rightarrow \boxed{\text{LIWV} = 1\,800 \text{ kV}} \end{aligned}$$

#### A.3.3.3 HV bridge transformer neutral point (star)

Protective arrester: T – A'

$$\begin{aligned} \text{SIPL} &= 1\,071 \text{ kV} \\ \text{RSIWV} &= 1,15 \times 1\,071 \text{ kV} = 1\,232 \text{ kV} && \Rightarrow \boxed{\text{SIWV} = 1\,600 \text{ kV}} \\ &&& \Rightarrow \boxed{\text{LIWV} = 1\,800 \text{ kV}} \end{aligned}$$

#### A.3.3.4 HV bridge transformer phase-to-earth (delta)

Protective arrester: CM+V3

$$\begin{aligned} \text{SIPL} &= 706 \text{ kV} + 395 \text{ kV} = 1\,101 \text{ kV} \\ \text{RSIWV} &= 1,15 \times 1\,101 \text{ kV} = 1\,266 \text{ kV} && \Rightarrow \boxed{\text{SIWV} = 1\,300 \text{ kV}} \\ &&& \Rightarrow \boxed{\text{LIWV} = 1\,550 \text{ kV}} \end{aligned}$$

#### A.3.3.5 LV bridge transformer phase-to-earth (star)

Protective arrester: ML+V

$$\begin{aligned} \text{SIPL} &= 435 \text{ kV} + 395 \text{ kV} = 830 \text{ kV} \\ \text{RSIWV} &= 1,15 \times 830 \text{ kV} = 955 \text{ kV} && \Rightarrow \boxed{\text{SIWV} = 1\,050 \text{ kV}} \\ &&& \Rightarrow \boxed{\text{LIWV} = 1\,300 \text{ kV}} \end{aligned}$$

#### A.3.3.6 LV bridge transformer phase-to-earth (delta)

Protective arrester: E+V3

$$\begin{aligned} \text{SIPL} &= 263 \text{ kV} + 395 \text{ kV} = 658 \text{ kV} \\ \text{RSIWV} &= 1,15 \times 658 \text{ kV} = 757 \text{ kV} && \Rightarrow \boxed{\text{SIWV} = 750 \text{ kV}} \\ &&& \Rightarrow \boxed{\text{LIWV} = 950 \text{ kV}} \end{aligned}$$

### A.3.4 Smoothing reactor withstand voltages

#### A.3.4.1 Pole line smoothing reactors

The worst case for the stresses between the terminals of pole line smoothing reactors is given by the slow-front overvoltages on the DC side, which is limited by the arrester (DL).

SIPL of arrester (DL):	1 328 kV
Maximum DC voltage:	816 kV
Sum of both voltages:	2 144 kV
Smoothing reactors:	300 mH
Transformer inductances:	176 mH
Total inductance:	476 mH

$$\text{Voltage between terminals: } 2\,144 \text{ kV} \times (150 \text{ mH} / 476 \text{ mH}) = 676 \text{ kV}$$

Since two 75 mH reactors are used in series for the pole line smoothing reactor, and one DR arrester is connected in parallel for each smoothing reactor, the withstand voltages of the smoothing reactor is defined by the DR arrester.

For the design of the smoothing reactor arrester (DR) the following values for co-ordination currents are chosen:

SIPL	=	641 kV	at 3 kA
LIPL	=	719 kV	at 10 kA

Impulse withstand voltage of single reactor:

RSIWV	=	$1,15 \times 641 \text{ kV}$	=	737 kV	⇒	<span style="border: 1px solid black; padding: 2px;">SIWV = 750 kV</span>
RLIWV	=	$1,20 \times 719 \text{ kV}$	=	863 kV	⇒	<span style="border: 1px solid black; padding: 2px;">LIWV = 950 kV</span>

#### A.3.4.2 Neutral bus smoothing reactors

SIPL of arrester (E):	263 kV
Maximum DC voltage:	82 kV
Sum of both voltages:	345 kV
Smoothing reactors:	300 mH (MR operating mode)
Transformer inductances:	176 mH
Total inductance:	476 mH
Voltage between terminals:	$345 \text{ kV} \times (150 \text{ mH} / 476 \text{ mH}) = 165 \text{ kV}$

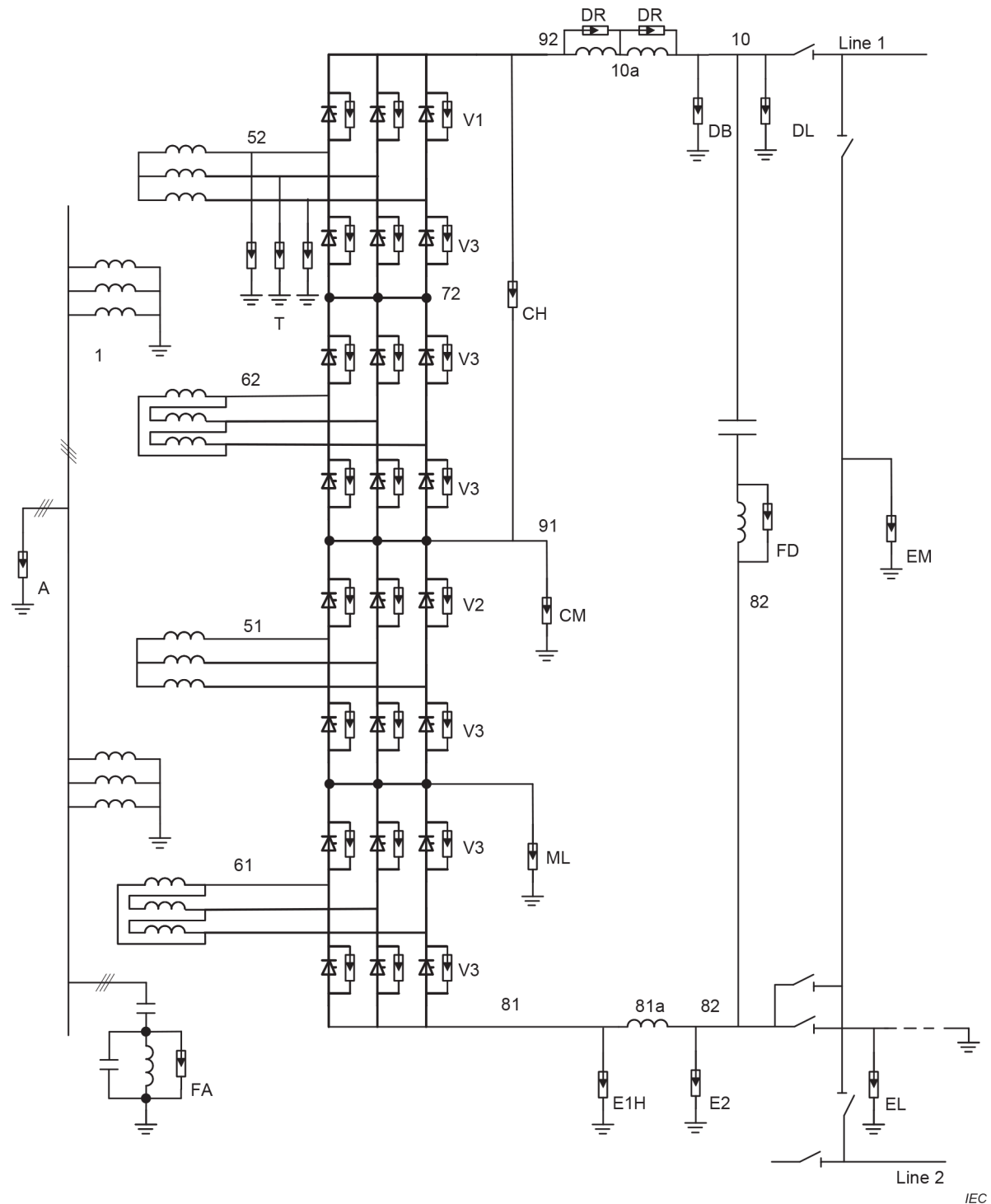
As for arrester E, the following values for co-ordination currents are chosen:

SIPL	=	263 kV	at 1 kA
LIPL	=	301 kV	at 10 kA

Impulse withstand voltage of reactor (150 mH):

RSIWV	=	$1,15 \times 263 \text{ kV}$	=	301 kV	⇒	<span style="border: 1px solid black; padding: 2px;">SIWV = 375 kV</span>
RLIWV	=	$1,20 \times 301 \text{ kV}$	=	361 kV	⇒	<span style="border: 1px solid black; padding: 2px;">LIWV = 450 kV</span>

A.3.5 Results



Arrester type		A	T	V1	V2	V3	ML	CM	CH	D	E1H	E2	DR
$U_{ch}$ or CCOV	kV	318ac	885	245	245	245	245	477	477	816	50dc +80ac	50dc	>40ac
LIPL	kV	913	1344	395	395	395	435	791	791	1579	320	320	719
Coordination Current	kA	20	0.6	2.4	1.2	0.6	0.6	5	5	10	20	20	10
SIPL	kV	780	1344	395	395	395	435	706	706	1328	263	263	641
Coordination Current	kA	2	1	4	2	1	1	1	1	1	1	1	3
Energy capability	MJ	8,9	9	10	5	2,6	2,8	4,6	4,6	9	3,6	3,6	2,0

Protection location	1	51	61	71	52	62	72	81	82	91	92	10
$U_{ch}$ or CCOV(kV)	318 rms	477	245	245	886	710	710	50dc +80ac	50 dc	477	880	816 dc
LIPL (kV)	907	--	--	435	1 344	--	--	320	320	791	--	1 579
SIPL (kV)	1550	1 300	950	750	1 800	1 550	1 550	450	450	1 175	1 800	1 950
LIWV (kV)	780	830	631	435	1 344	1 101	1 101	263	263	706	1 344	1 328
SIWV (kV)	1 175	1 050	750	550	1 600	1 300	1 300	325	325	950	1 600	1 600

Protection location	51, 61 ph-ph	51-61	81-91	52, 62 ph-ph	52-62	91-92	92-10a	81-82	valve
LIP (kV)	--	--	--	--	--	740	719	--	395
LIWV (kV)	750	1 175	1 175	750	1 175	1 175	1 050	450	454
SIPL (kV)	473	790	706	473	790	706	641	263	395
SIWV (kV)	650	950	950	650	950	950	950	375	454

**Figure A.6 – AC and DC arresters (LCC HVDC converter station in a pole with two 12-pulse converters in series)**

## Bibliography

IEC Guide 108, *Guidelines for ensuring the coherence of IEC publications – Horizontal functions, horizontal publications and their application*

IEC 60060-1, *High-voltage test techniques – Part 1: General definitions and test requirements*

IEC 60071-1:2019, *Insulation co-ordination – Part 1: Definitions, principles and rules*

IEC 60071-2:2018, *Insulation co-ordination – Part 2: Application guidelines*

IEC 60071-5:2014, *Insulation co-ordination – Part 5: Procedures for high-voltage direct current (HVDC) converter stations*

IEC 60099-5:2018, *Surge arresters – Part 5: Selection and application recommendations*

IEC 60099-9:2014, *Surge arresters – Part 9: Metal-oxide surge arresters without gaps for HVDC converter stations*

IEC 60505:2011, *Evaluation and qualification of electrical insulation systems*

IEC 60617, *Graphical symbols for diagrams, available at <http://std.iec.ch/iec60617>*

IEC 60700-1:2015/AMD1:2021<sup>3</sup>, *Thyristor valves for high voltage direct current (HVDC) power transmission – Part 1: Electrical testing*

IEC 60721-3-0:2020, *Classification of environmental conditions – Part 3: Classification of groups of environmental parameters and their severities. Introduction*

IEC TS 60815-1:2008, *Selection and dimensioning of high-voltage insulators intended for use in polluted conditions – Part 1: Definitions, information and general principles*

IEC TS 60815-2:2008, *Selection and dimensioning of high-voltage insulators intended for use in polluted conditions – Part 2: Ceramic and glass insulators for a.c. systems*

IEC TS 60815-3:2008, *Selection and dimensioning of high-voltage insulators intended for use in polluted conditions – Part 3: Polymer insulators for a.c. systems*

IEC TR 60919-2:2008/AMD1:2015/AMD2:2020<sup>4</sup>, *Performance of high-voltage direct current (HVDC) systems with line-commutated converters – Part 2: Faults and switching*

IEEE. Bibliography on overvoltage protection and insulation co-ordination of HVDC converter stations, 1979-1989. *IEEE Transactions on Power Delivery*. 1991, 6(2), 744-753

IEEE. Insulation Coordination Designs of HVDC Converter Installations. *IEEE Transactions on Power Apparatus and Systems*. 1979, PAS-98(5), 1761-1776

IEEE. Modeling guidelines for fast-front transients. *IEEE Transactions on Power Delivery*. 1996, 11(1), 493–506

<sup>3</sup> A consolidated version of this document exists, comprising IEC 60700-1:2015 and IEC 60700-1:2015/AMD1:2021.

<sup>4</sup> A consolidated version of this document exists, comprising IEC TR 60919-2:2008, IEC TR 60919-2:2008/AMD1:2015 and IEC TR 60919-2:2008/AMD2:2020.



Canadian Electrical Association. *Performance of Metal Oxide Gapless Surge Arresters for HVDC Systems: Phase I*. Report 214 T 565, September 1990

CIGRE. *Application guide for insulation coordination and arrester protection of HVDC converter stations*. 33.05, Electra No. 96. Paris: CIGRE, 1984, 101-156

CIGRE. *Guide to procedures for estimating the lightning performance of transmission lines*. CIGRE technical brochure No. 63. Paris: CIGRE, 2021

CIGRE. *Guidelines for representation of network elements when calculating transients*. CIGRE technical brochure No. 39. Paris: CIGRE

CIGRE. *Guidelines for the application of metal-oxide arresters without gaps for HVDC converter stations*. CIGRE 33/14.05, publication 34. Paris: CIGRE, 1989

Elahi, H. et al. Insulation coordination process for HVDC converter stations: preliminary and final designs. *IEEE Transactions on Power Delivery*. 1989, 4(2), 1037-1048

EPRI. AC Transmission Line Reference Book – 200 kV and above, Third Edition Palo Alto, CA: EPRI, 2005

EPRI. *Handbook for insulation coordination of high-voltage DC converter stations*. EPRI Report No. EL-5414. Palo Alto, CA: EPRI, 1987

EPRI. Insulation coordination (chapter 11). In: *High-voltage direct current handbook*. EPRI Publication no. TR-104166. Palo Alto, CA: EPRI, 1994

Jonsson, T. and Björklund P-E, *Capacitor commutated converters for HVDC*. SPT PE 02-03-0366 IEEE/KTH. Stockholm Power Tech. Conference, June 1995

Melvold, D. DC arrester test philosophies on recent HVDC projects as used by various suppliers. *IEEE Transactions on Power Delivery*. 1991, 6(2), 672-679

Sadek, K. et al. Capacitor commutated converter circuit configurations for d.c. transmission. *IEEE Transactions on Power Delivery*. 1998, 13(4), 1257-1264

---

IEEE. Bibliography on overvoltage protection and insulation co-ordination of HVDC converter stations, 1979-1989. *IEEE Transactions on Power Delivery*. 1991, 6(2), 744-753

IEEE. Insulation Coordination Designs of HVDC Converter Installations. *IEEE Transactions on Power Apparatus and Systems*. 1979, PAS-98(5), 1761-1776.

IEEE. Modeling guidelines for fast-front transients. *IEEE Transactions on Power Delivery*. 1996, 11(1), 493–506.

Canadian Electrical Association. *Performance of Metal Oxide Gapless Surge Arresters for HVDC Systems: Phase I*. Report 214 T 565, September 1990.

CIGRE. *Application guide for insulation coordination and arrester protection of HVDC converter stations*. 33.05, Electra No. 96. Paris: CIGRE, 1984, 101-156

CIGRE. *Guide to procedures for estimating the lightning performance of transmission lines*. CIGRE technical brochure No. 63. Paris: CIGRE, 2021.

CIGRE. *Guidelines for representation of network elements when calculating transients*. CIGRE technical brochure No. 39. Paris: CIGRE.

CIGRE. *Guidelines for the application of metal-oxide arresters without gaps for HVDC converter stations*. CIGRE 33/14.05, publication 34. Paris: CIGRE, 1989.

Elahi, H. et al. Insulation coordination process for HVDC converter stations: preliminary and final designs. *IEEE Transactions on Power Delivery*. 1989, 4(2), 1037-1048

EPRI. AC Transmission Line Reference Book – 200 kV and above, Third Edition Palo Alto, CA: EPRI, 2005.

EPRI. *Handbook for insulation coordination of high-voltage DC converter stations*. EPRI Report No. EL-5414. Palo Alto, CA: EPRI, 1987.

EPRI. Insulation coordination (chapter 11). In: *High-voltage direct current handbook*. EPRI Publication no. TR-104166. Palo Alto, CA: EPRI, 1994.

Jonsson, T. and Björklund P-E, *Capacitor commutated converters for HVDC*. SPT PE 02-03-0366 IEEE/KTH. Stockholm Power Tech. Conference, June 1995.

Melvold, D. DC arrester test philosophies on recent HVDC projects as used by various suppliers. *IEEE Transactions on Power Delivery*. 1991, 6(2), 672-679

Sadek, K. et al. Capacitor commutated converter circuit configurations for d.c. transmission. *IEEE Transactions on Power Delivery*. 1998, 13(4), 1257-1264

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