Aarul Jain

Flat No. 137, Pocket K
Sarita Vihar, New Delhi-110076, India
Tel. No.: +91 9871632880

E-Mail: aaruljain@gmail.com
aaruljain@synopsys.com

SHORT BIO

Aarul Jain is a TUV-SUD Certified Professional (Level-2) for ISO26262 and IEC61508 and a Synopsys Functional Safety Expert. He has 20+ years of experience in semiconductor industry in multiple roles. He started his career in architecture and design of Digital IPs and SoCs and then transitioned into the role of Functional Safety Manager in 2016. Currently, he is managing the SoC frontend design team and leading Functional Safety for System Solutions Group at Synopsys. Previously, he lead and managed a team of 12 safety architects and safety managers at NXP Semiconductors (Noida and Bangalore) to develop ISO26262 and IEC61508 compliant microcontrollers. Aarul was also responsible for managing the NXP Safeassure program and driving NXP functional safety strategy for customer enablement. He has 7 patents and 5 publications in international conferences.

EXPERIENCE SUMMARY (20+ YRS)

- Synopsys India Private Limited, Noida, India — Nov 23 – Present
  Senior Director – System Solution Group
- NXP Semiconductors, Noida, India — Jun 11 – Nov 23
  Senior Manager – Functional Safety, MCU/MPU Engineering
- CSR plc (now Qualcomm), Phoenix, AZ, USA — Dec 09 – June 11
  RTL Design Engineer – DSP Group
- Intel Corporation, Chandler, AZ, USA — Jan 08 – Dec 08
  Graduate Research Assistant – Ultra Mobility Group
- Freescale Semiconductors (now NXP Semiconductors), Noida, India — Jun 04 – Aug 07
  Senior Design Engineer (IC-II) – Core Technology Group, WMSG

EDUCATION

- Arizona State University, Tempe, AZ — Aug 07 – Dec 09
  MS, Electrical Engineering (Major: VLSI Signal Processing)
- NSIT, University of Delhi, India — Aug 00 – Jun 04
  B.E., Electronics & Communication Engineering

FUNCTIONAL SAFETY EXPERIENCE

- Certified ISO26262 and IEC61508 TUV-SUD Professional Engineer. Recognized Functional Safety Expert and was member of NXP Patent Committee. Consistently top rated employee (6 times in last 8 years).
- Advised senior management on organization changes to establish a high performing safety team and a strong safety culture across the global organization.
- Established Functional Safety Team in India and enabled the growth of NXP India Functional Safety Expert Community across different Product Lines from grounds-up to 24 safety engineers in 4 years.
- Responsible for ISO26262 compliance and developing safety work products for S32 Automotive Platform and PowerPC (MPC5xxx) based automotive microcontrollers as Functional Safety Manager.
  - Developing System Safety Concept and MCU Safety Architecture for HW developed as SEooC.
  - Guiding the team to perform Safety Analysis (FMEDA, DFA, FTA) and author the safety manual.
  - Responsible for Impact Analysis, Safety Plan, Managing Audit and Assessments, Safety Case.
  - Reviewer and approver of various safety work products.
  - Working with tool vendors such as Ansys to improve Safety Analysis framework for semiconductors.
  - Delivered on-time high quality results for more than 18 ISO26262 compliant SoCs over 7 years.
- Development of Safety Collaterals for LPC55S3x - NXP's first MCU targeted for Industrial Safety Applications based on IEC61508.
- Responsible for reinvigorating and managing the Safeassure Program to establish strong customer focus for functional safety in the organization.

- Responsible for driving NXP Safety Strategy with focus on customer support and enablement.
- Demonstrated thought-leadership in supporting customer facing teams though trainings, education programs and hands-on workshops.
- Reduced average response time for customer queries from 108 days to less than 12 days while supporting more than 50 customers (OEM and Tier1) and resolving about 300 support requests annually.
- Won the top most award from NXP CEO for exhibiting Total Quality Mindset.

- Development of System Safety Concepts for Reference Designs/Product Demonstrators.
  - Authoring requirements for the MCU HW used in ASIL-D High-Voltage BMS Reference Design.
  - Responsible for updating System Safety Concept for ASIL-D EV Traction Inverter Reference Design.
  - Responsible for developing System Safety Concept for ASIL-B Sunroof Anti-Pinch demonstrator.
- Skills: Medini Analyze (FMEDA), Isograph RWB(FTA), Cameo Systems Modeler(SysML), Simulink

ARCHITECTURE AND DESIGN EXPERIENCE

- Managing frontend design team (RTL Design and Signoff, SoC Verification) in Systems Solution Group at Synopsys.
- SoC Architecture and Integration for NXP's Vybrid Platform:- Responsible for clocking and low-power architecture, interconnect performance and integration of various IP modules.
- IP Design for CSR's GPS Products:- Design, synthesis and integration of various IP (DSP Filters, Interpolators, Quantizers, Mixers, Memory Interfaces, RF interface) for SirfStarV GPS/Glonass Receiver.
- Synthesis and Verification of Intel's Langwell SoC for Moorestown platform:- Verification of boot flow and verification and synthesis of various IPs for Langwell SOC.
- High Performance Compute Algorithm Mapping to Nvidia's CUDA:- Implementation of iterative methods for solving sparse linear equations in C/C++ on Compute Unified Device Architecture(CUDA).
- Development of Starcore based DSP Platform for Baseband Platforms:- RTL Design and micro-architecture of L1 Memory Subsystem and bus interface for Starcore140 DSP platform. Implementations of assembly routines for power save and restore for Starcore 3400 DSP platform.
- Skills: Verilog, VCS, Design Compiler, PrimeTime, LEC, C/C++, Amba Designer, SystemC, SystemVerilog.

PATENTS

- Aarul Jain, Ashu Gupta, Hemant Nautiyal, "Method and Apparatus for Fault Aggregation based on Fault Reaction with Virtualization Support", 2022 [Filed]
- Ankush Sethi, Rohit Kaul, Aarul Jain, "Method and Apparatus for selective IO Safe-stating for independent on-chip Safety Applications", 2022 [Filed]
- Arvind Kaushik, Aarul Jain, Nishant Jain, "Address Fault Detection System", US011853157B2, 2023
- Aditya Khandelwal, Aarul Jain, Rupesh Chaturvedi, "A Safe Radar System by Insertion and Detection Virtual Target", 2021 [Filed]
- Aarul Jain, Dirk Wendel, "Memory error detection system", US9727408B2, 2015
- Deboleena Minz Sakalley, Rakesh Pandey, Neha Agarwal, Aarul Jain, "Data strobe signal generation for flash memory", US9251906B1, 2013.
- Aarul Jain, Rohit Patel, Rakesh Pandey, "Single Cycle Dual Port Memory Using Single Port Memory Bank", US9129661B2, 2013

CONFERENCES/PUBLICATIONS

- Aarul Jain, "Application and Trends of Functional Safety for Semiconductors", VLSID 2022.
- Aarul Jain, Aviral Shrivastava, Chaitali Chakrabarti, "A Latency Aware Replacement Policy for Process Tolerant Caches", International Conference on VLSI Design, January 2011.
- Veera Papirla, Aarul Jain, Chaitali Chakrabarti, "Low Power Robust Signal Processing", International Symposium on Low Power Electronics and Design, pp 303-306, Aug 2009.
- Aarul Jain, "Zero-Latency Predictive Synchronizer", http://ip.com/IPCOM/000223857, Def. Pub., Dec. 2012.
- Dhananjay V. Gadre & Aarul Jain, "Lifetime Counter using AVR", Circuit Cellar AVR-Contest Jun 2004.
- Aarul Jain & Dhananjay V. Gadre, "Gameboy Advance for Non-Gaming Applications", Dr. Dobb's Journal, May 2004.